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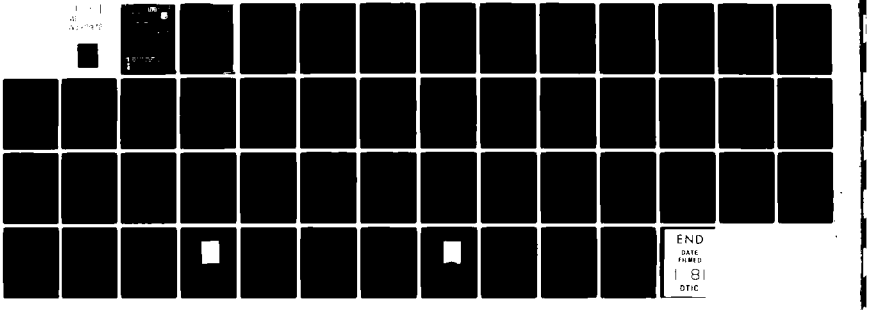

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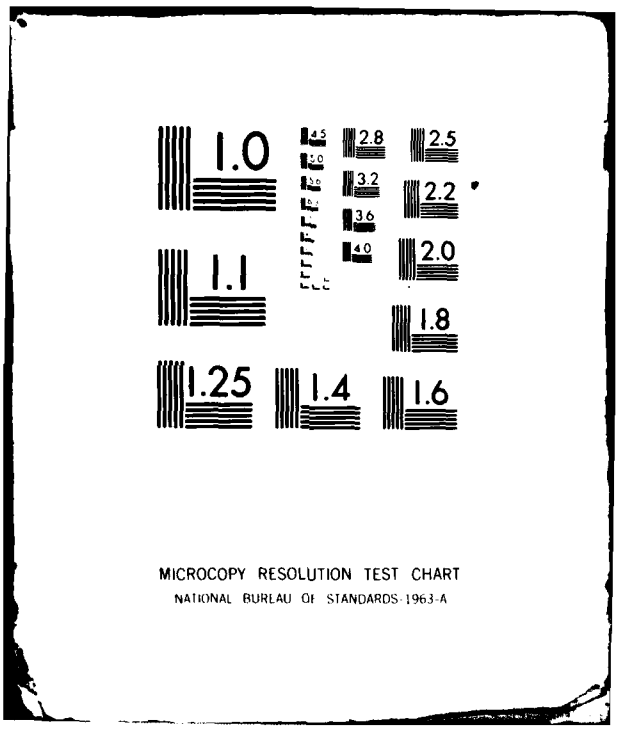
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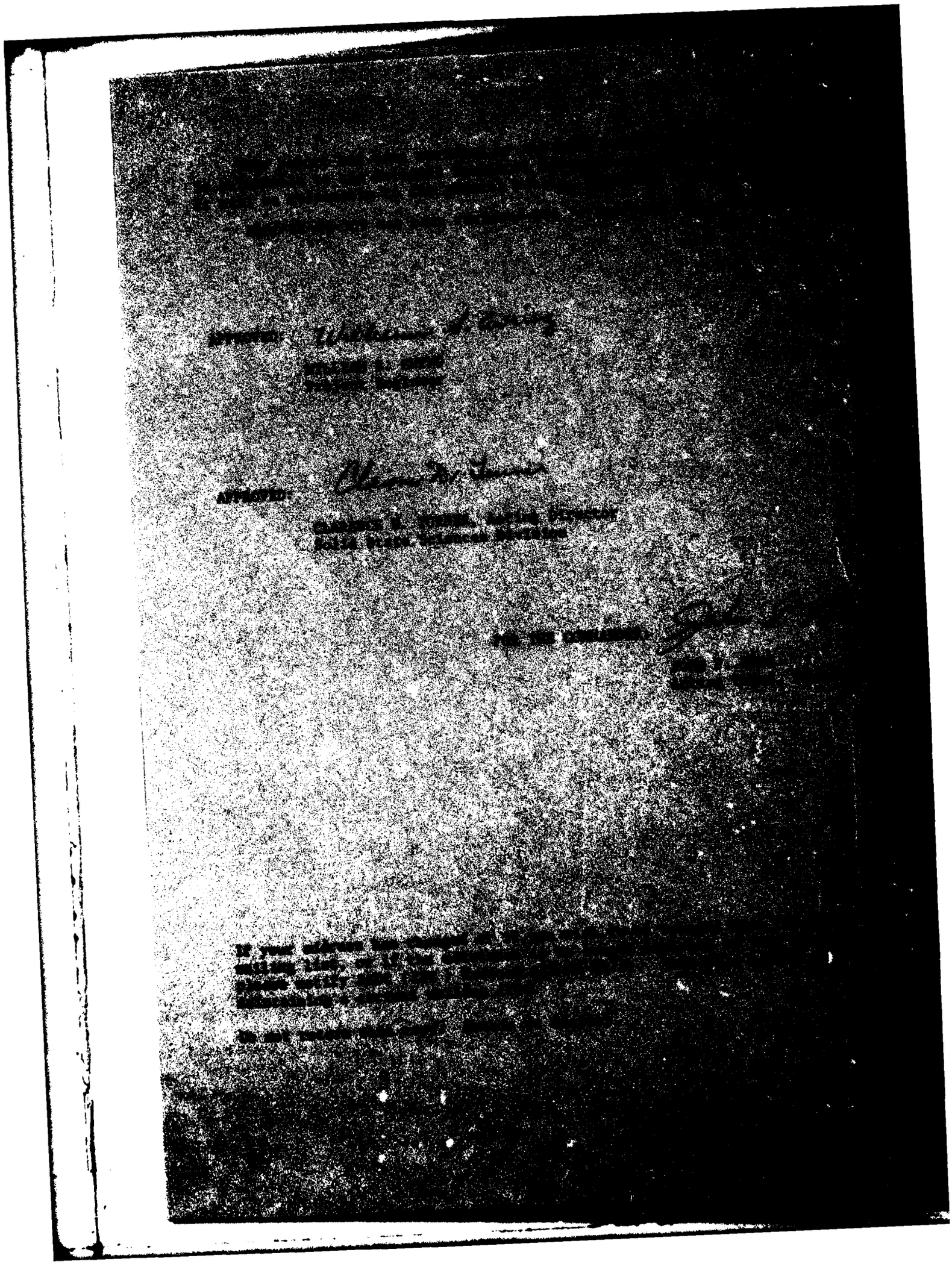

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This report discusses the design and modeling of CCD split-gate filter structures, both surface-channel and buried-channel. It also includes initial design of recursive filter structures which can be implemented without the use of op amps in either CCD or switched-capacitor form.

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SECTION 1

INTRODUCTION AND SUMMARY

This is the first interim report on contract F19628-79-C-0176, CCD Applications Study.

The technical studies on this program were scheduled to begin with an investigation of the design and modeling of CCD filters. To meet these goals we have concentrated on two activities:

1. A study of conventional CCD split-gate filter structures, both surface-channel and buried-channel.
2. An investigation of high-speed recursive filter structures which can be implemented without the use of op amps.

Initial work on both activities consisted of preparing theoretical models for the various filter structures. We have also designed some recursive filter test structures and incorporated them into the test area on a CCD development chip. The first wafers of these devices have recently been received from processing and preliminary testing has now begun.

SECTION 2

SPLIT-GATE FILTER STRUCTURES

In collaboration with John Pennock* at Southampton University, England, we have been carrying out a comprehensive analysis of split-gate filter structures with the object of building up a set of computer programs for designing this type of device.

SURFACE-CHANNEL DEVICES

A detailed study of the working of the floating-gate output as used in split-electrode filters has been carried out with particular attention being given to the inherent depletion-capacitance-induced distortion. The analysis starts with the case of a single unsplit sense gate; current and voltage sensing are distinguished and the dc transfer characteristic is used to deduce the low-frequency distortion. The analysis is then extented to the case of a split-gate structure; for voltage sensing the movement of charge perpendicular to the direction of charge propagation to equalize the surface potential under the two parts of the split gate is included. This is known as "charge hogging"[1,2]

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*While in England, D. R. Lamb was the supervisor of Mr. Pennock's PhD program.

[1] C. P. Traynar, et al., "Depletion-Capacitance-Induced Distortion in Surface-Channel CCD Transversal Filters," IEE J. Solid State and Electron Devices, 1, 73, 1977.

[2] K. R. Hense and T. W. Collins, "Linear Charge-Coupled Device Signal Processing Techniques," IEEE Trans., Vol. ED-23, No. 265, 1976.

and has not previously been quantitatively analyzed. Finally the single-gate analysis is carried over to the case of a complete filter to enable computer simulation of the entire device. The passage along the filter of signal charge packets corresponding to an input sine wave of abritrary frequency can be simulated; the distorted output is calculated as a function of time and the harmonic content of the output extracted. To illustrate the use of these programs some examples are given below.

Figure 1 shows the contours of distortion versus input signal amplitude Q_{pk} and bias level Q_{dc} for a single floating gate using current sensing. V_{GO}' is the effective gate voltage given by

$$V_{GO} - V_{FB} \text{ and } V_o = \frac{\varepsilon_o \varepsilon_s Q N_A}{C_{ox}^2}$$

For voltage sensing the distortion characteristics are exactly the same when normalized to take into account the capacitive loading caused by the high-input impedance voltage follower and any stray capacitance. Thus, voltage sensing with a bias voltage V_{GO}' and total load capacitance ratio $C_s/C_{Gate} = R$ is equivalent to current sensing with a gate voltage $V_{GO}'R/(R + 2)$ and with a larger signal charge packet of $Q_{sig}(R + 2)/(R + 1)$. In practice C_s is usually deliberately increased with a load capacitor so the performance is not unduly degraded by a small R value.

Figure 2 shows the intrinsic small signal tap-weight error that arises with voltage sensing on a split-gate structure for various R values; that is, various capacitive loads. This occurs because changing the tap weight not only changes the amount of signal charge that is monitored, but also the ratio of depletion and load capacitance and thus sensitivity to this charge.

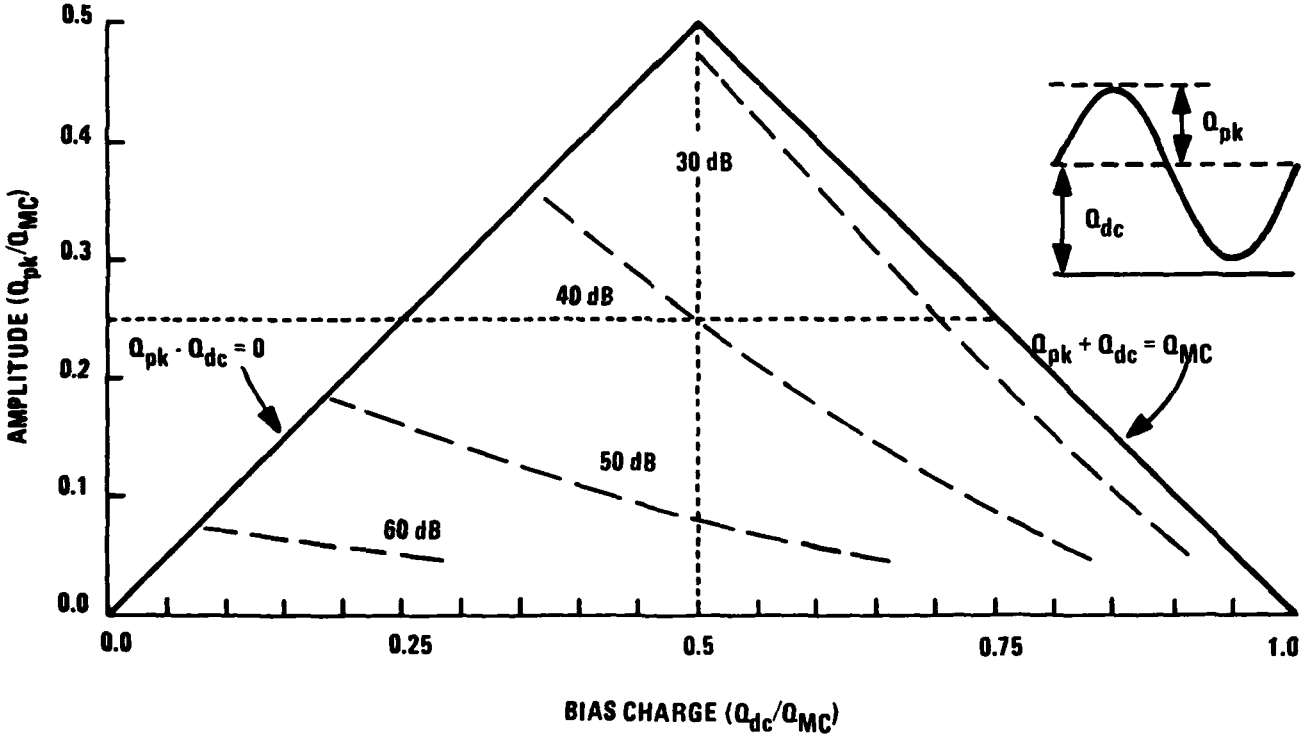

Figure 1. Current Sensing: Contours of Distortion vs Input Signal Amplitude Q_{pk} and Bias Level Q_{dc} ($V_{GO}'/V_o = 30$)

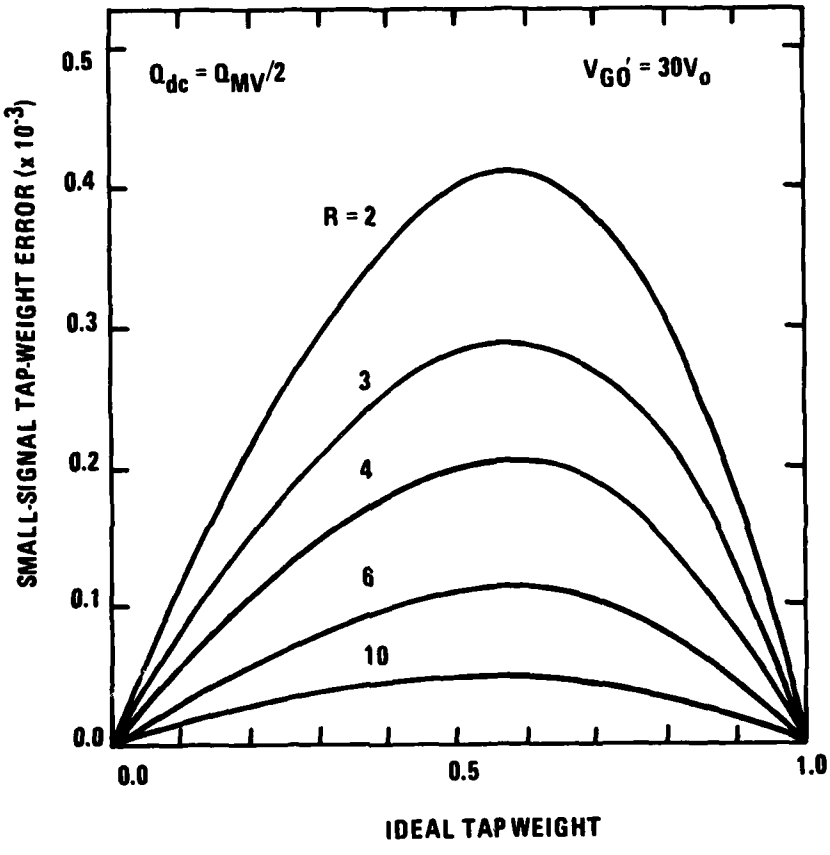

Figure 2. Single Split-Gate Voltage Sensing: Small Signal Tap-Weight Error vs Ideal Tap Weight for Various R = $C_s/A_G C_{ox}$

For each R the greatest error occurs with a tap weight of ≈ 0.58 and this error increases as R decreases, that is, as the gate loading decreases. The maximum error is also a function of gate bias voltage and of the bias level of the signal. This latter effect makes it impossible to correct for the error by adjusting the position of the split in the gate and gives rise to distortion.

The final examples show simulations of a 63-tap low-pass filter designed using the Parks-McLellan algorithm ($F_p/F_c = 0.1$, $F_s/F_c = 0.131$, and $\delta_1/\delta_2 = 1$). The gate area is 300 μm x 10 μm, oxide thickness = 0.11 μm, $N_A = 10^{15}$ cm^{-3}, $V_{GO}' = 5$V (effective gate bias $V_{GO} - V_{FB}$), and the maximum charge handling capability $Q_{MC} = 5$ pc.

Figure 3 shows current sensing, Figure 4 shows voltage sensing with different values of load capacitance, and Figure 5 shows voltage sensing including charge-hogging effects.

BURIED-CHANNEL DEVICES

No analysis of the buried-channel floating-gate output has been published; because of the nonlinear dependence of channel voltage against signal charge, this structure has been widely held to introduce more distortion than a surface-channel device (for example, Reference 3). The analysis

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[3] R.W. Broderson, C.R. Hewes, and D.D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE J. Solid State Circuits, Vol. SC-11, No. 75, 1976.

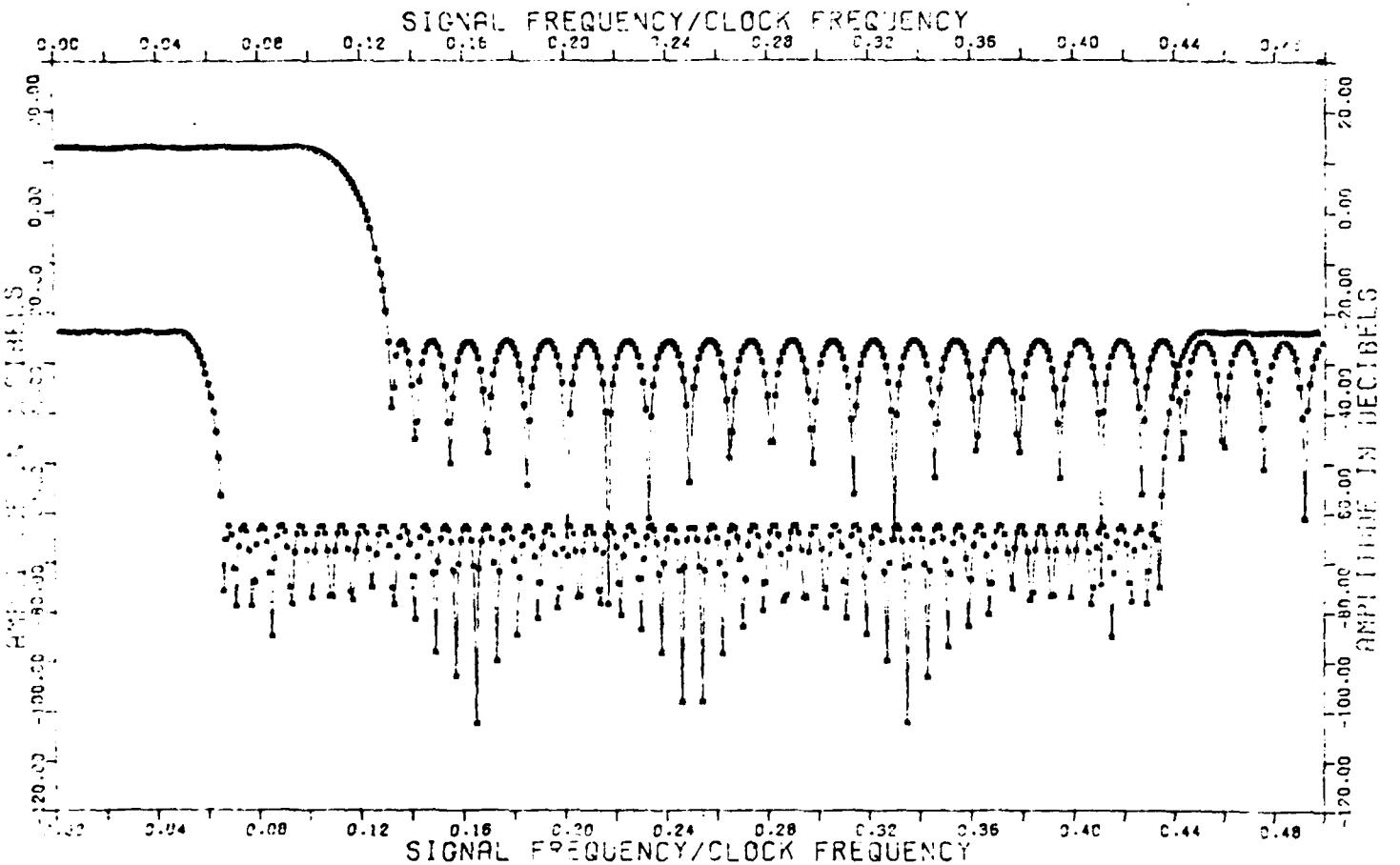


Figure 3. Fundamental and Second Harmonic Responses of Filter: Current Sensing ($V_{GO'}$ = 5V, V_o = 1/6V, $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$, Q_{MC} = 5 pc, 0 dB = 1 pc amplitude)

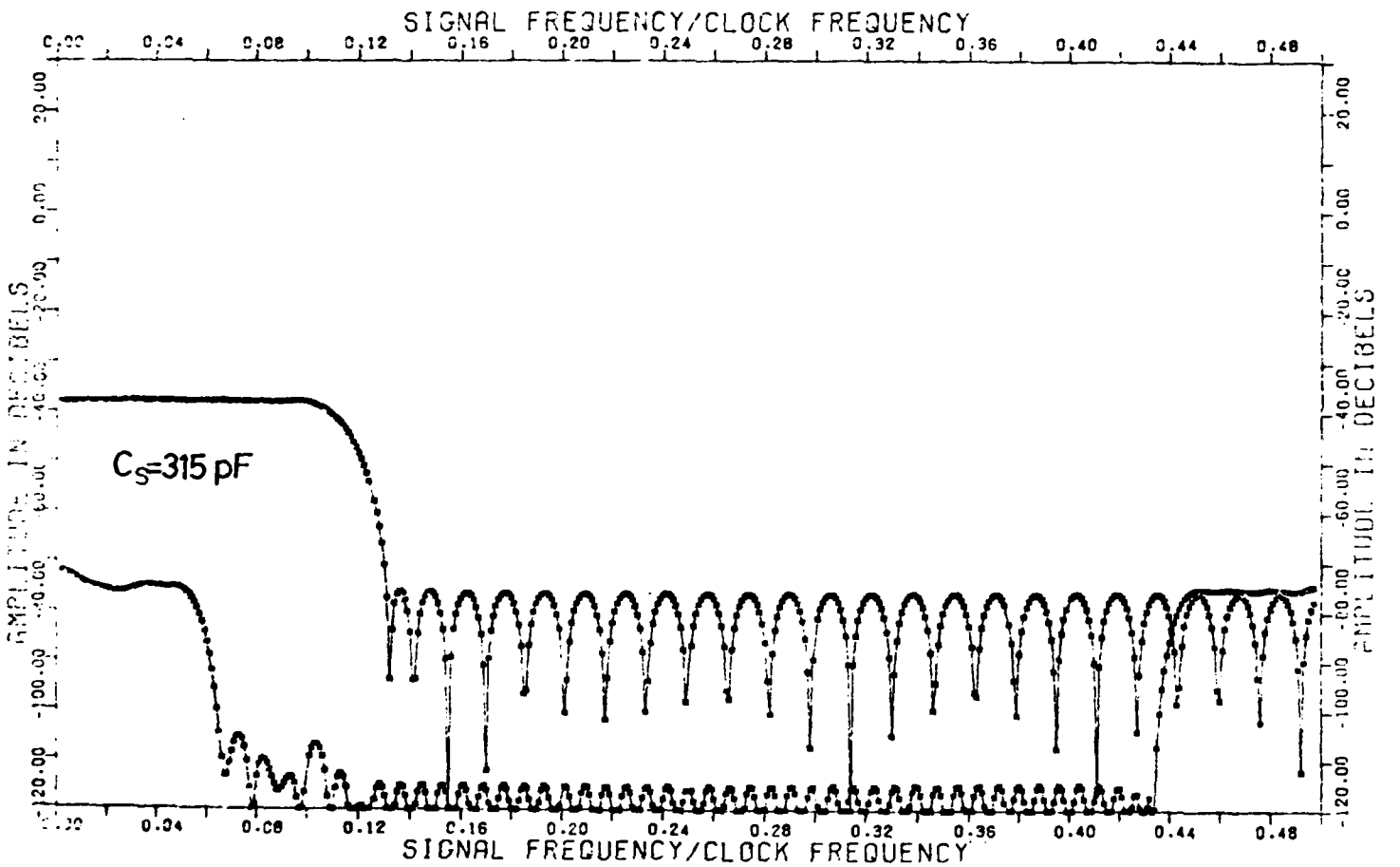


Figure 4a. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Linear Charge Input ($V_{GO}' = 5V$, $V_o = 1/6V$, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, $C_{ox} = 1$ pF, 0 dB = 1V amplitude)

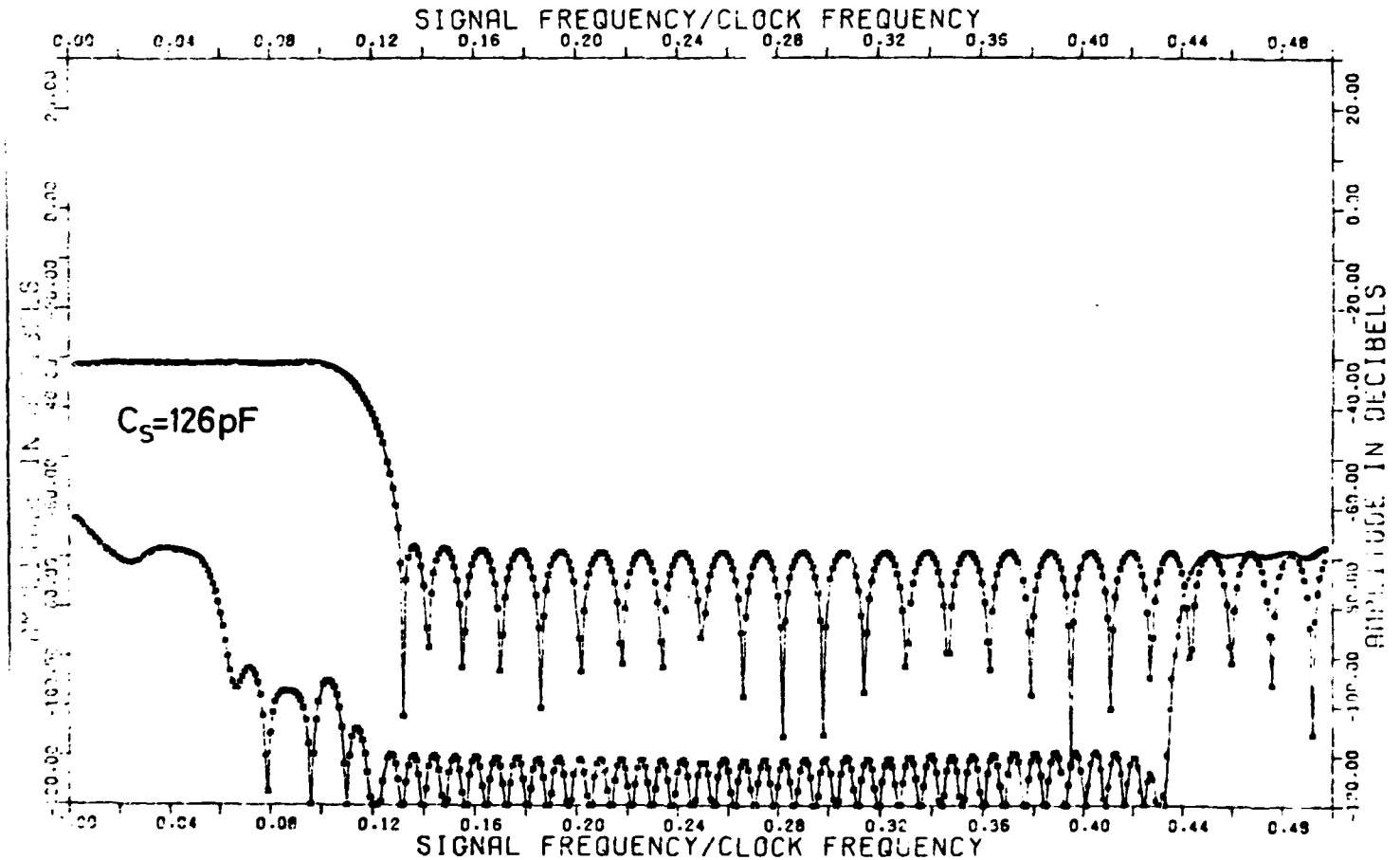


Figure 4b. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Linear Charge Input (V_{GO}' = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

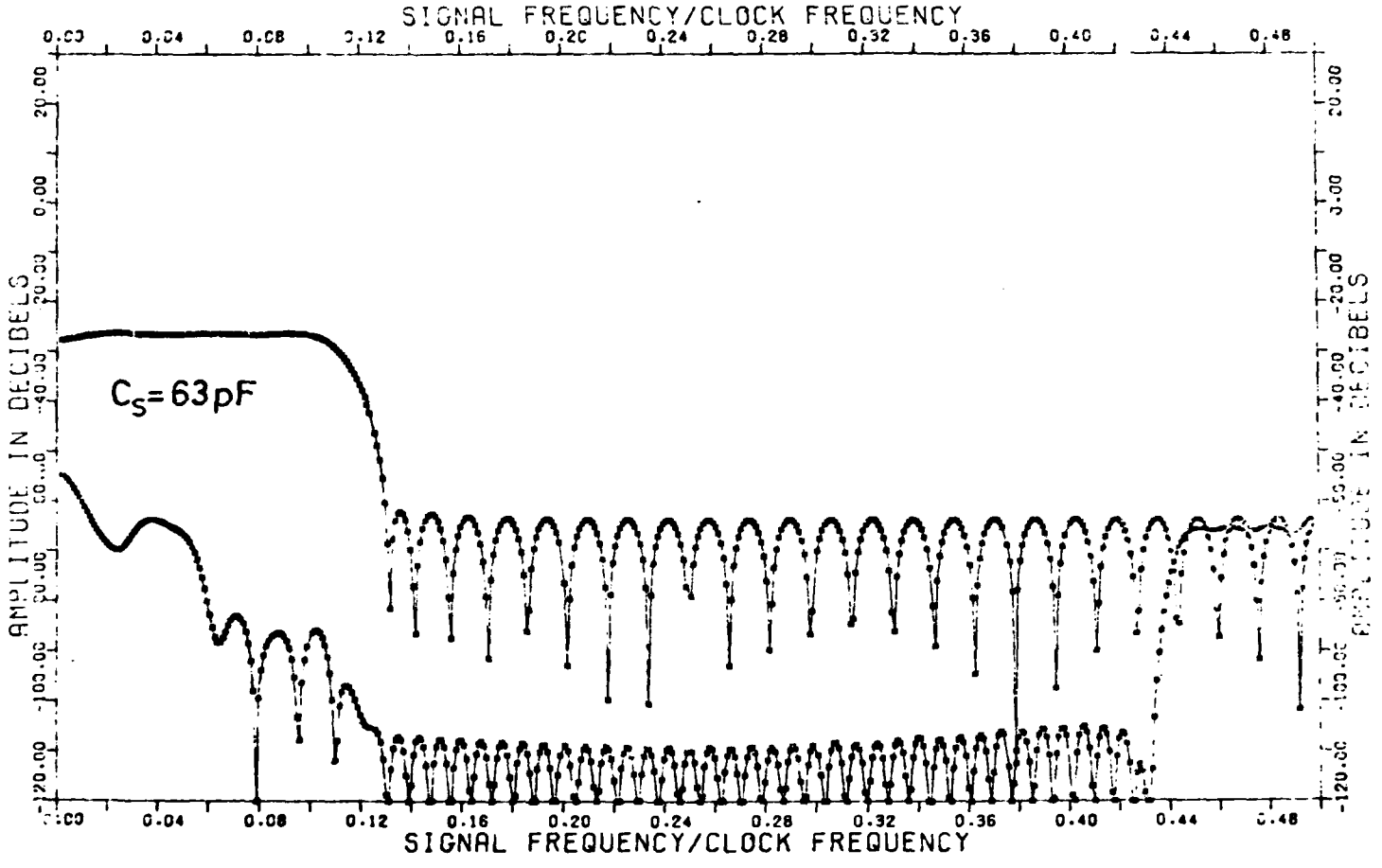


Figure 4c. **Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Linear Charge Input (V_{GO}' = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)**

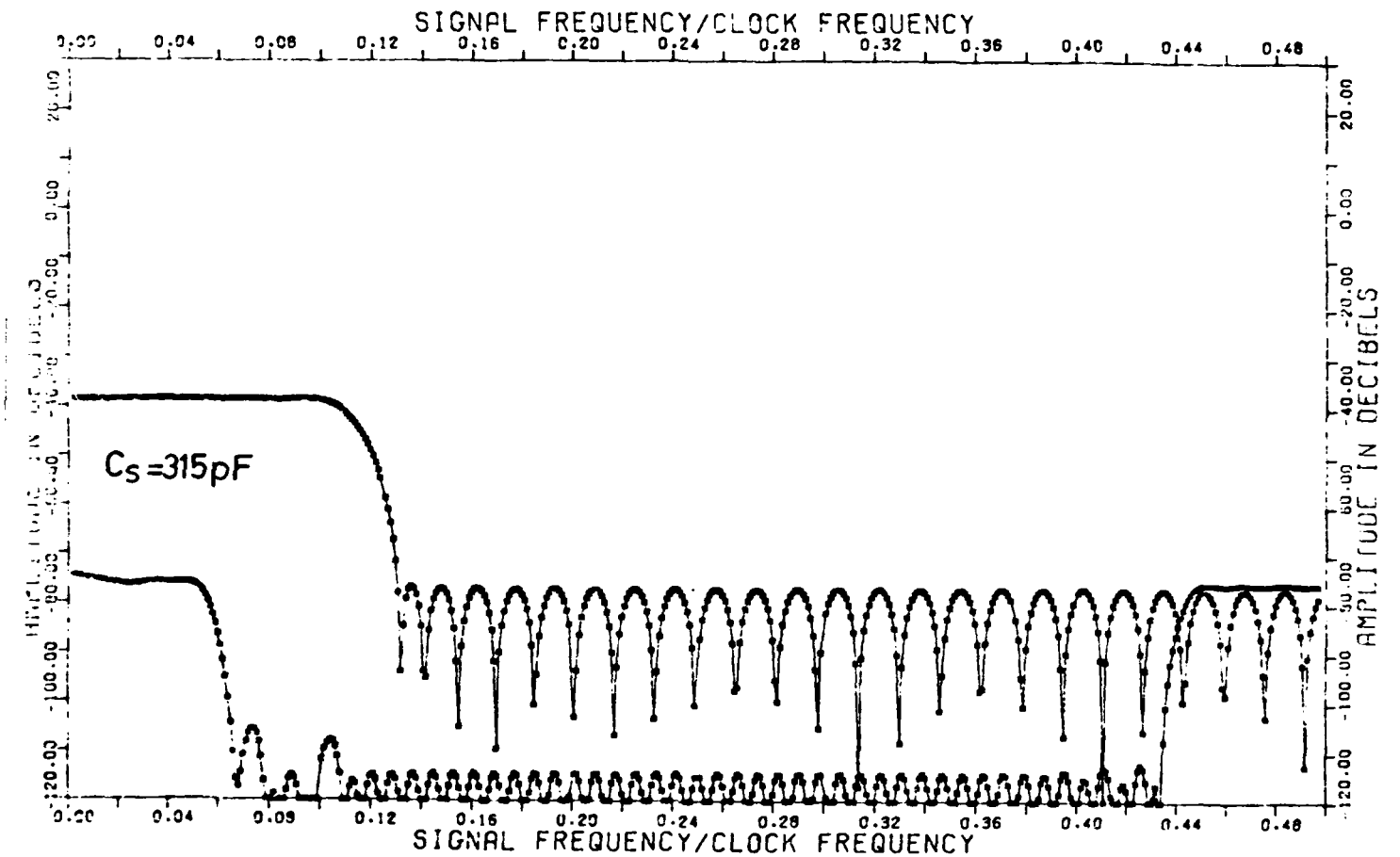


Figure 5a. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Including Charge-Hogging, Linear Charge Input (V_{GO}' = 5V, V = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

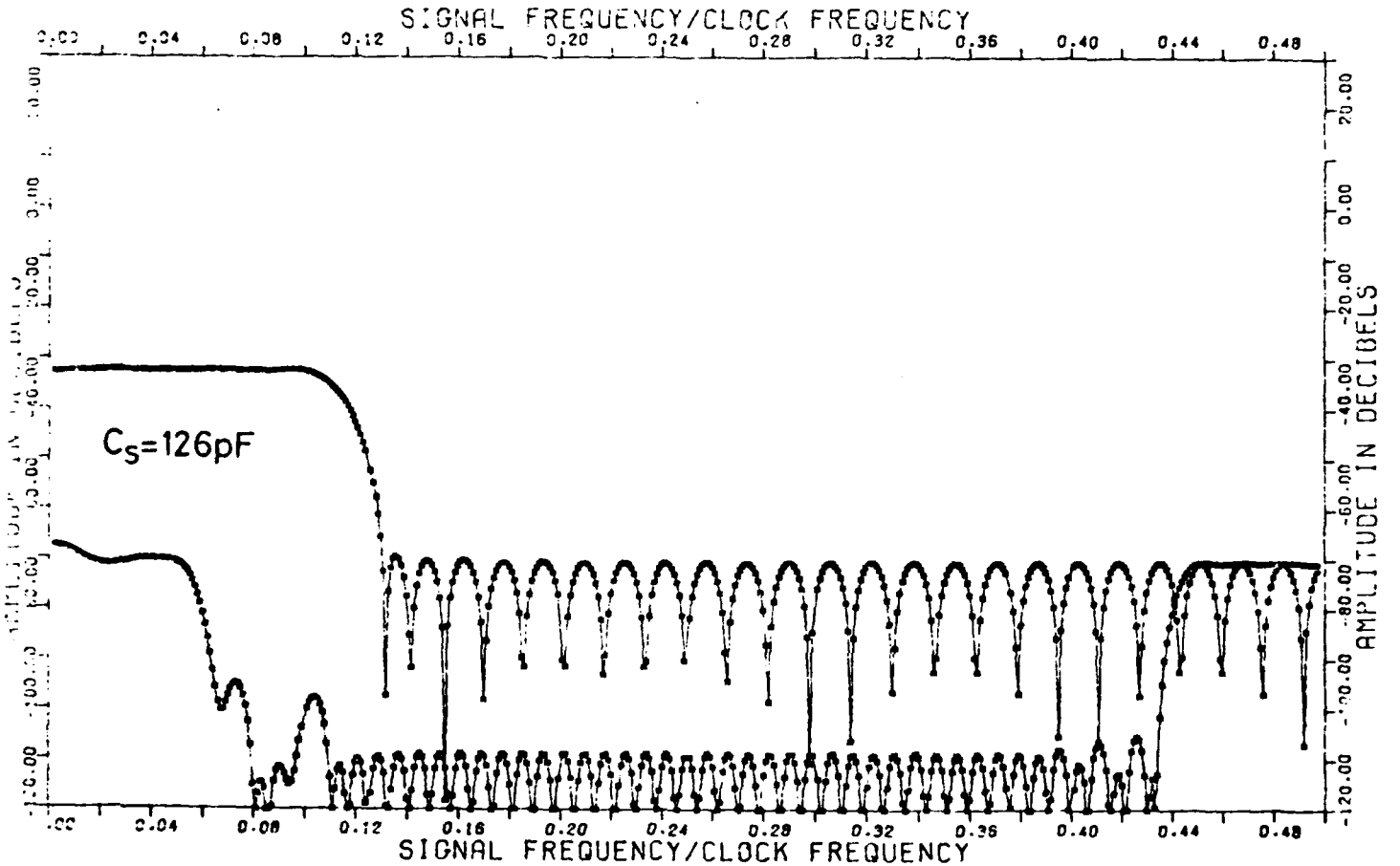


Figure 5b. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Including Charge-Hogging, Linear Charge Input (V_{GO}' = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

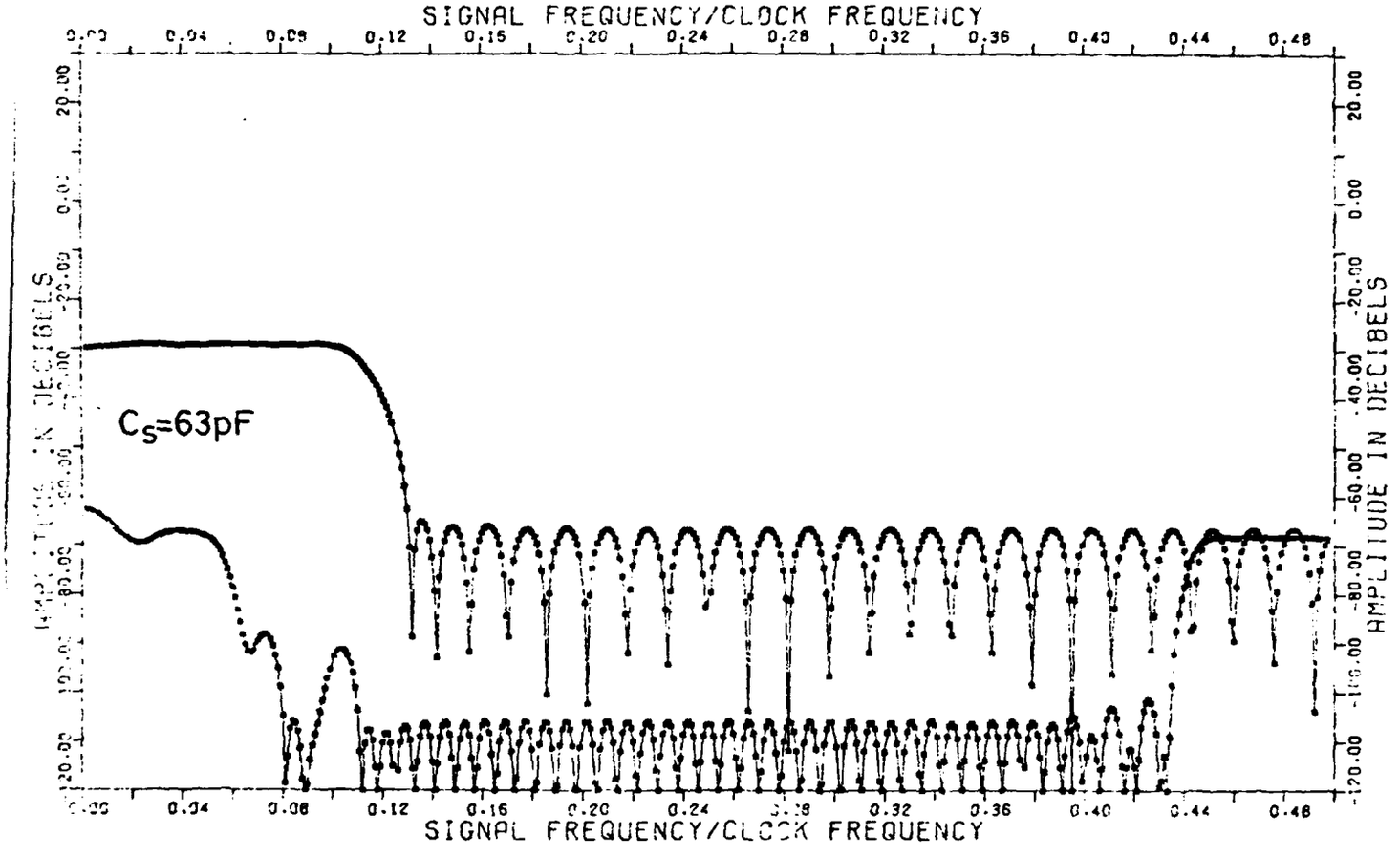


Figure 5c. Fundamental and Second Harmonic Responses of Filter: Voltage Sensing Including Charge-Hogging, Linear Charge Input (V_{GO}' = 5V, V_o = 1/6V, $Q_{pk} = Q_{MV}/4$, $Q_{dc} = Q_{MV}/2$, C_{ox} = 1 pF, 0 dB = 1V amplitude)

of the buried-channel structure is more complex than that for a surface-channel device and there is no convenient normalization to enable results to be generalized to cover all possible doping profiles and signal levels. However, by taking a range of reasonable doping levels, typical distortion levels can be derived and the performance compared with surface-channel devices.

The analysis was started using the case of structures with a rectangular doping profile in the channel region. Again a single-gate output was analyzed first for both current and voltage sensing schemes. The results obtained were then compared with those for a Gaussian doping profile and finally a complete filter was again simulated to obtain the frequency dependence of the distortion.

Examples of this analysis are demonstrated in Figures 6 and 7, which show the harmonic distortion as a function of surface doping level in a Gaussian doping profile for both current and voltage sensing. The input sine wave was chosen to have amplitude $V_G C_{ox}/10$ and dc level $V_G C_{ox}$; that is, $Q_{MC}/4$ and $Q_{MC}/2$, where $Q_{MC} = 0.4\ V_S C_{ox}$ and is a generous estimate of the charge-handling capability of a buried-channel device. A comparison of Figures 6 and 7 with Figure 1 is interesting since the latter figure shows that a similarly operated surface-channel device has an output distortion of 40 dB below fundamental. Thus for the range of parameters shown the depletion-capacitance-induced distortion for buried-channel devices is actually less than for surface-channel devices.

One other point should, however, be borne in mind. In the case of surface-channel devices $\Delta Q_G = C_{ox}\ \Delta\psi_s$, where $\Delta\psi_s$ is the change in surface potential

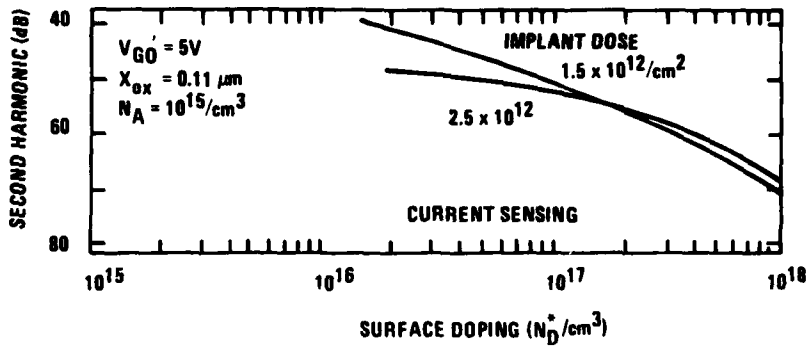


Figure 6. Harmonic Distortion (dB below fundamental) vs Surface Doping for Gaussian Doping Profile (current sensing) ($Q_{pk} = V_{GO}'C_{ox}/10$, $Q_{dc} = V_{GO}'C_{ox}/5$)

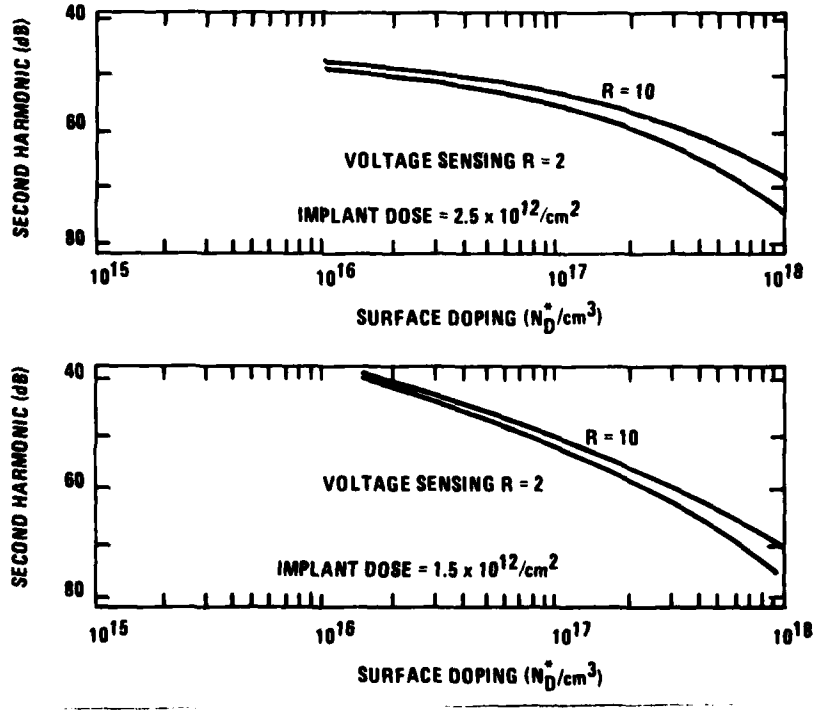


Figure 7. Harmonic Distortion (dB below fundamental) vs Surface Doping for Gaussian Doping Profile (voltage sensing) ($Q_{pk} = V_{GO}'C_{ox}/10$, $Q_{dc} = V_{GO}'C_{ox}/5$)

caused by the introduction of the signal charge. Any input scheme which sets this surface potential linearly with respect to the input voltage would yield an overall linear transfer function. The diode cut-off input scheme ideally achieves this and an output second harmonic 50 dB below the fundamental has been reported.[4] For a buried-channel device a diode cut-off input would set the channel potential rather than the surface potential and ΔQ_G does not vary linearly with the channel potential. In fact ΔQ_G is still equal to $C_{ox}\psi_s$ but there does not seem to be a simple input scheme for buried-channel devices which will achieve a linear input voltage conversion to $\Delta\psi_s$.

Figures 8, 9, and 10 show simulations of the 63-tap low-pass filter described previously. However, in this case a buried-channel implementation is assumed with a rectangular doping profile of $N_D = 2 \times 10^{16}$ cm^{-3}, $N_A = 10^{15}$ cm^{-3}, and oxide thickness 0.11 μm. As can be seen, the general level of distortion is very similar to that in a surface-channel device.

EFFECT OF TRANSFER INEFFICIENCY

In a CCD delay line transfer inefficiency, ϵ attenuates high-frequency signals and causes the time delay of the CCD to become frequency dependent. In a CCD filter these effects are compounded by the fact that the filter output depends on signal charges at all stages along the CCD; that is, the transfer inefficiency modifies the effective tap weights.

[4] C.H. Sequin, et al., "Self-Contained Charge-Coupled Split-Electrode Filters Using a Novel Sensing Technique" IEEE J. Solid-State Circuits, Vol. SC-12, No. 626, 1977.

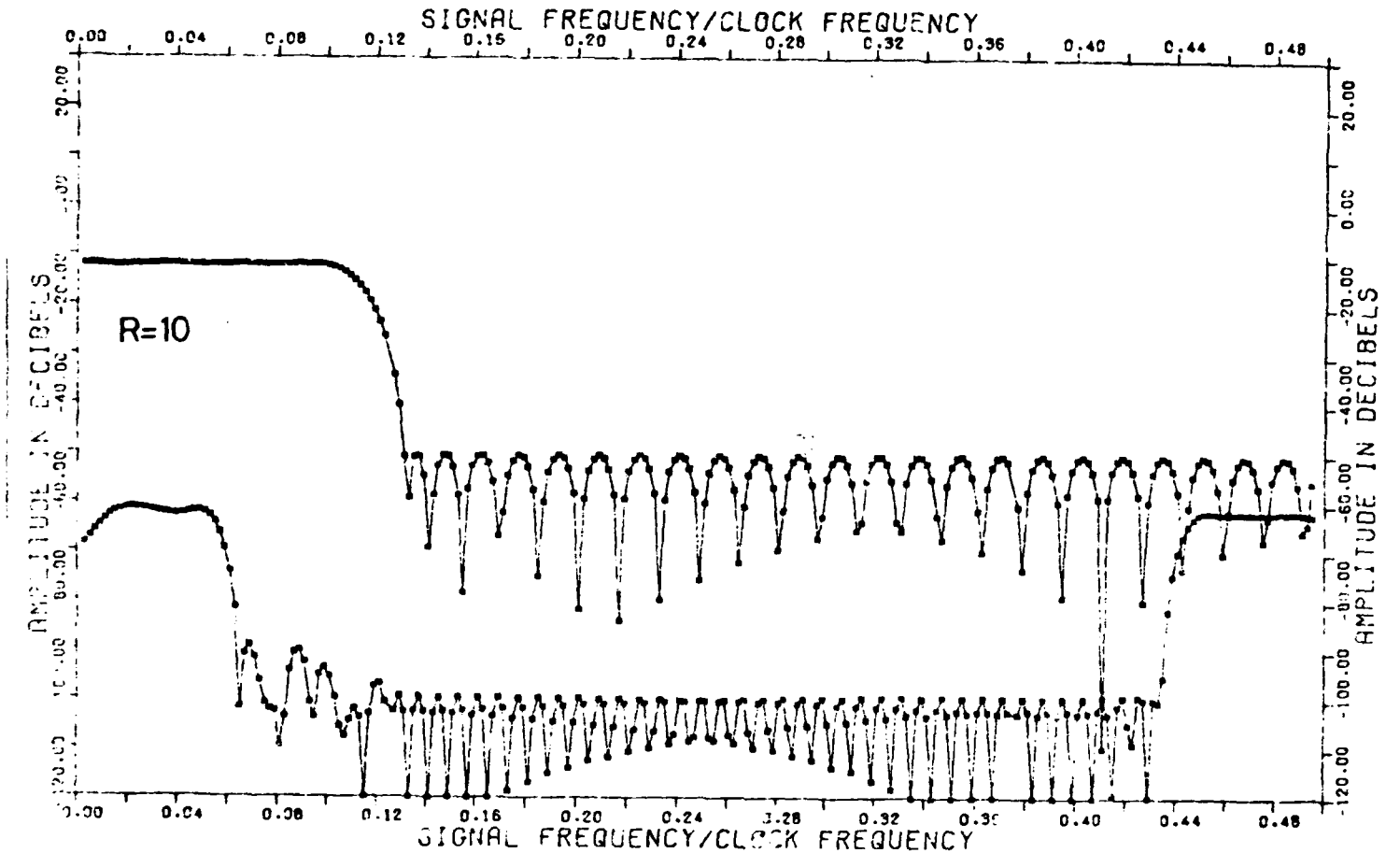


Figure 8. Fundamental and Second Harmonic for Buried-Channel Filter (N_D^* = $2 \times 10^{16}/cm^3$, $N_A = 10^{15}/cm^3$, $X_{ox} = 0.11$ μm, $X_j = 1$ μm, $V_{GO'} = 5V$, $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$)

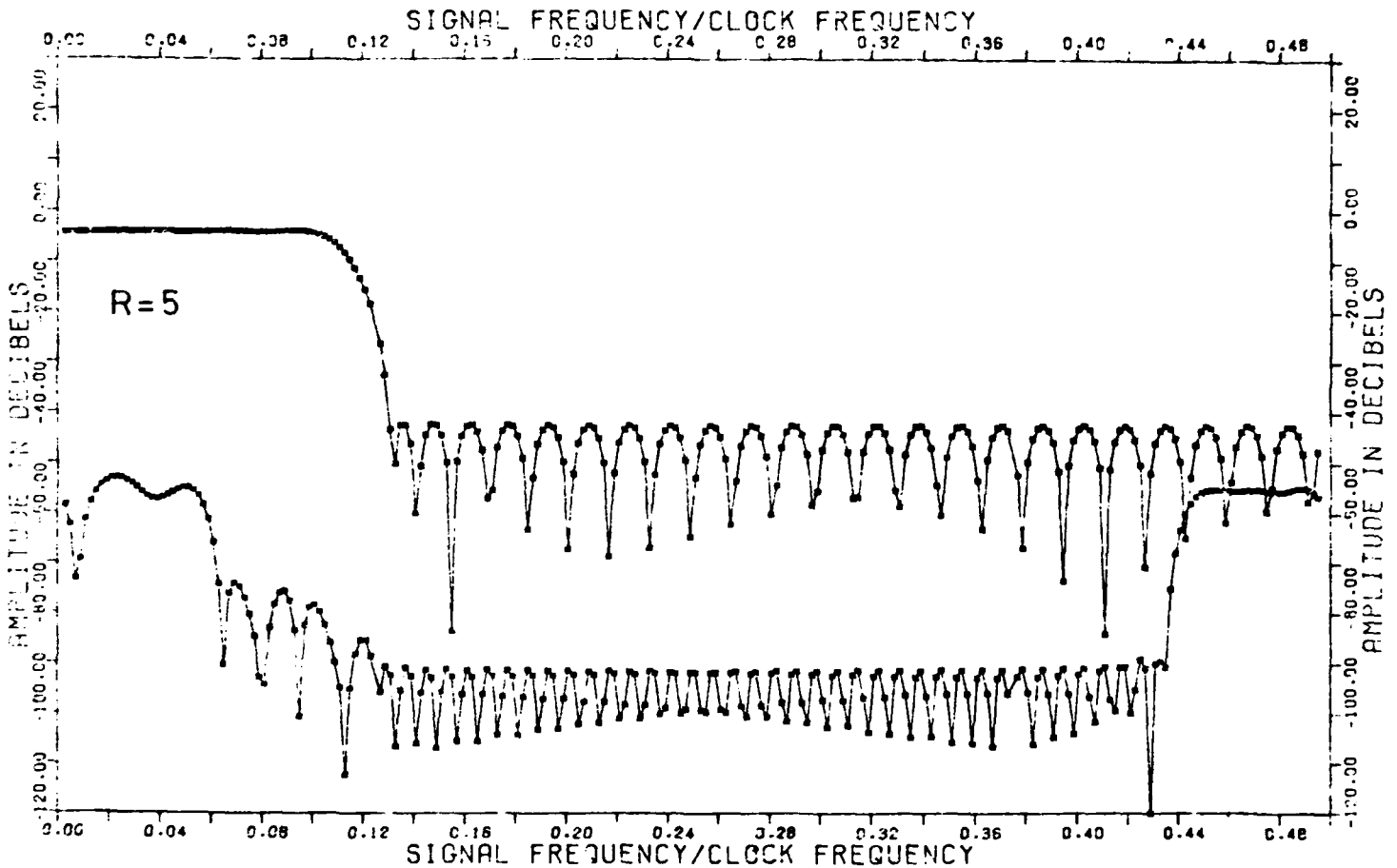


Figure 9. Fundamental and Second Harmonic for Buried-Channel Filter ($N_D{}^* = 2 \times 10^{16}/cm^3$, $N_A = 10^{15}/cm^3$, $X_{ox} = 0.11$ μm, $X_j = 1$ μm, $V_{GO}{}' = 5V$, $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$)

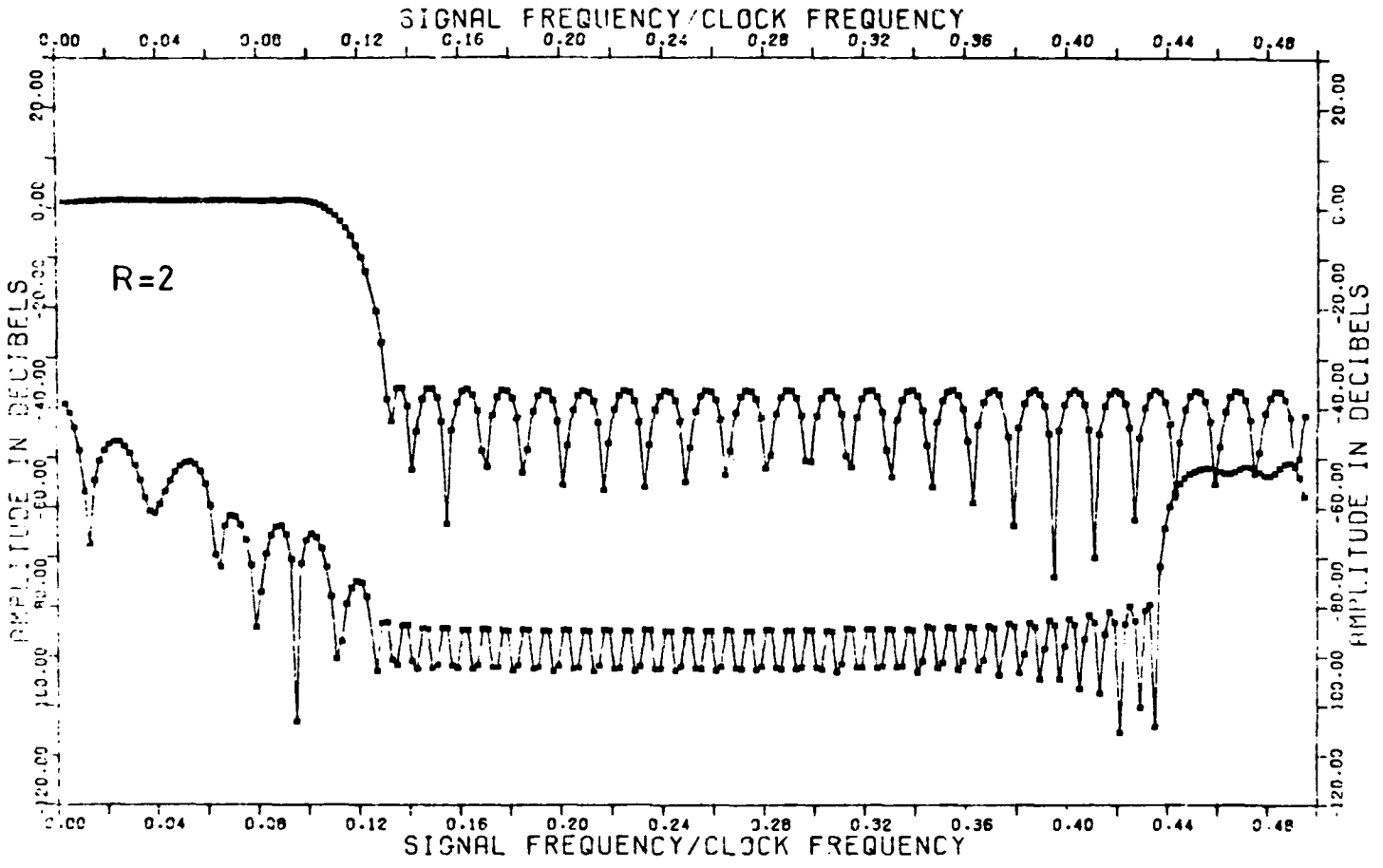


Figure 10. Fundamental and Second Harmonic for Buried-Channel Filter ($N_D^* = 2 \times 10^{16}/cm^3$, $N_A = 10^{15}/cm^3$, $X_{ox} = 0.11$ μm, $X_j = 1$ μm, $V_{GO'} = 5V$, $Q_{pk} = Q_{MC}/4$, $Q_{dc} = Q_{MC}/2$)

If ϵ is constant then the device is still ideally a linear system, so no harmonic distortion is introduced and only phase distortion occurs. In reality, however, ϵ is a function of the charge packet size and thus will give rise to harmonic distortion.

Consider an isolated charge packet injected into a N-stage CCD filter structure. In the absence of transfer inefficiency effects ($\epsilon = 0$ and $\alpha = 1 - \epsilon = 1$) the output as a function of time will scan the tap weights (h_i, $i = 0, \ldots, N - 1$) so that $Y(nT) = h_n$. If ϵ is not zero the charge packet will be progressively attenutated as it passes along the device and trailing packets will build up behind it. As the signal charge smears out, then, the output at any one time will be the weighted sum of several h_i and the impulse response will be altered to (h_i, $i = 0, \ldots, \infty$). The impulse response is now of infinite duration since even after many clock periods there will still be a very small fraction of the signal charge left in the device.

The modified impulse response h_i may be derived with reference to Figure 11, which is a flow chart of the charge packets through the CCD. Possible signal flow paths are represented by lines and each bit of the CCD is represented by a column since each clock period the charge moves one step: a fraction α of the charge at each node moves horizontally to the next bit on the right, the remainder, a fraction ϵ, is left behind and moves vertically downwards. The filter output will be

$$\sum_{i=0}^{N-1} q_i h_i$$

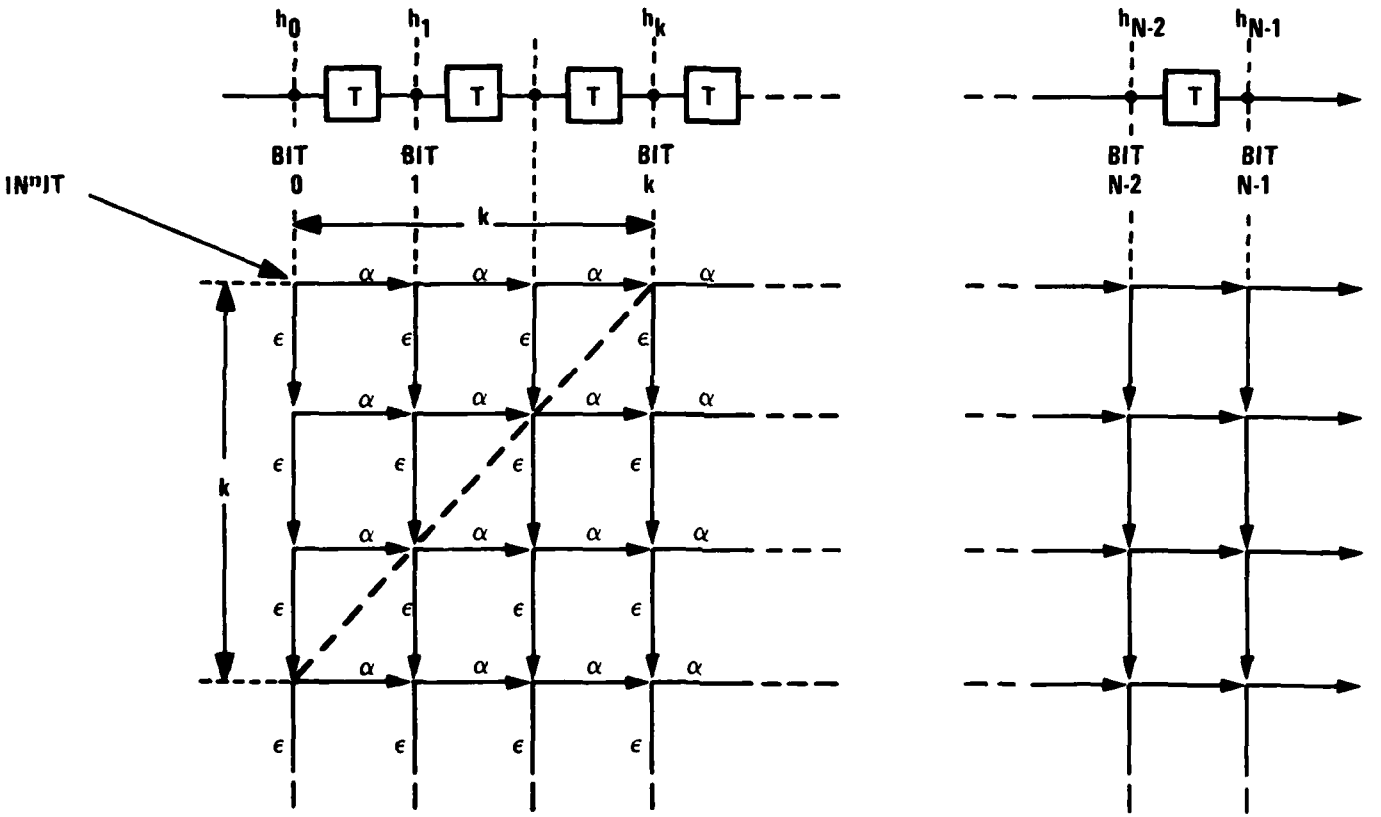


Figure 11. Signal Flow Graph of CCD Filter

where q_i is the total charge in the column corresponding to the i^{th} stage. If a single isolated charge packet of unit amplitude is injected into the device (top left) then k clock periods later the only nodes containing charge will be those on the dashed diagonal line. At such a node in the i^{th} column the charge present will be given by

$$q_i = \binom{k}{i} \alpha^i \epsilon^m \qquad i = 0, \ldots, k$$

where $m = k - i$. The modified impulse response is thus given by

$$h_k' = \sum_{i=0}^{k} h_i \binom{k}{i} \alpha^i \epsilon^{k-i} \qquad k = 0, 1, \ldots, \infty$$

This modification of the impulse response implies an alteration of the frequency response of the filter. The impulse response of a typical filter is shown in Figure 12; it has a central lobe of time duration $1/F_{co}$ where F_{co} is between F_p and F_s and is the approximate cut-off frequency. For very low-frequency signals ($< 1/NF_c$), at any given time, each element of the CCD contains approximately the same amount of signal charge. Most of the output will come from the central taps and there is very little cancellation of ac signals from different taps. For signals of frequency above F_{co}, several cycles will be caught within the central lobe: the net signal from the central lobe will be formed from the cancellation of many tap signals in the lobe and is thus likely to be comparable to the signal from the other tap weights. It is thus convenient to consider effects in the pass-band and stop-band separately.

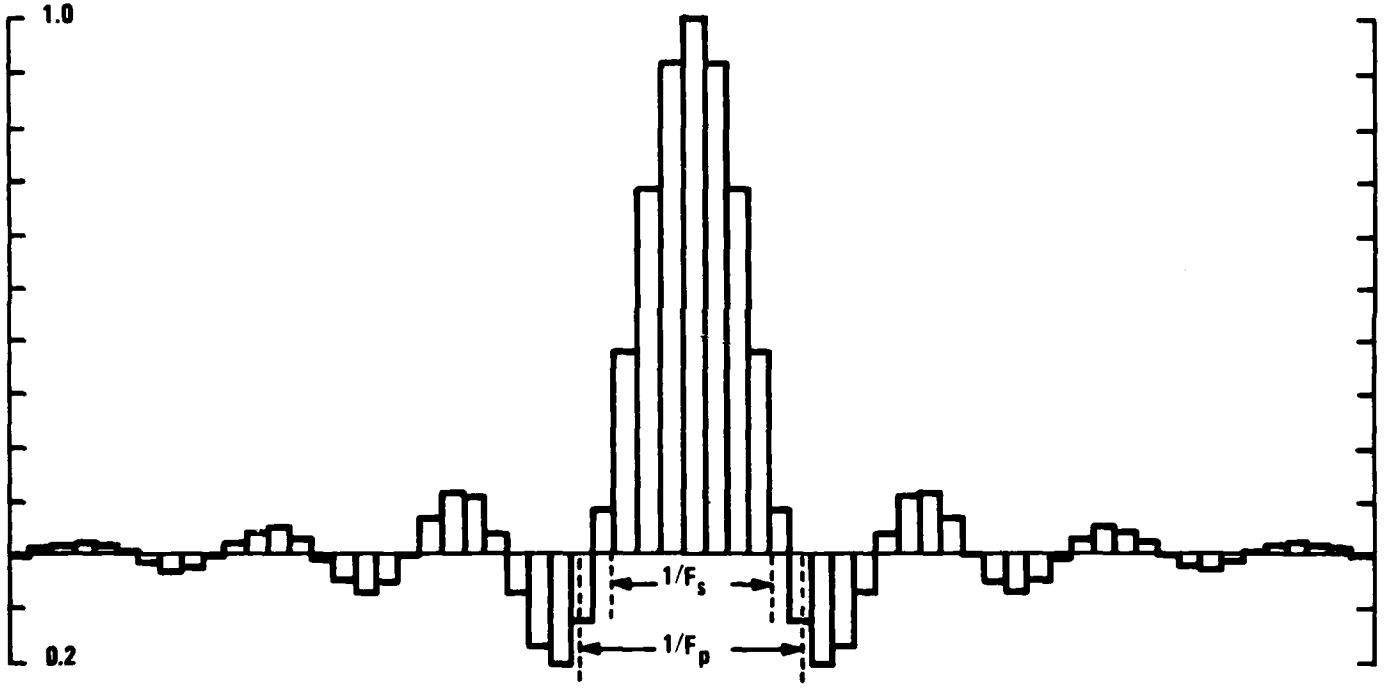


Figure 12. Impulse Response of a Typical Low-Pass Filter (Parks McClellan: $F = 0.100\ F_c$, $F_s = 0.131\ F_c$, $\delta_1/\delta_2 = 1$)

Pass-Band

In the pass-band most of the output signal comes from the central taps, where the charge packets have undergone about N/2 transfers. An approximate model for this situation is derived by replacing the inefficient filter by the series connection of a delay line of length N/2, with transfer inefficiency ϵ and a following perfect filter. The overall frequency response will then be the sum of the ideal frequency response and the low-pass function illustrated in Figure 13.

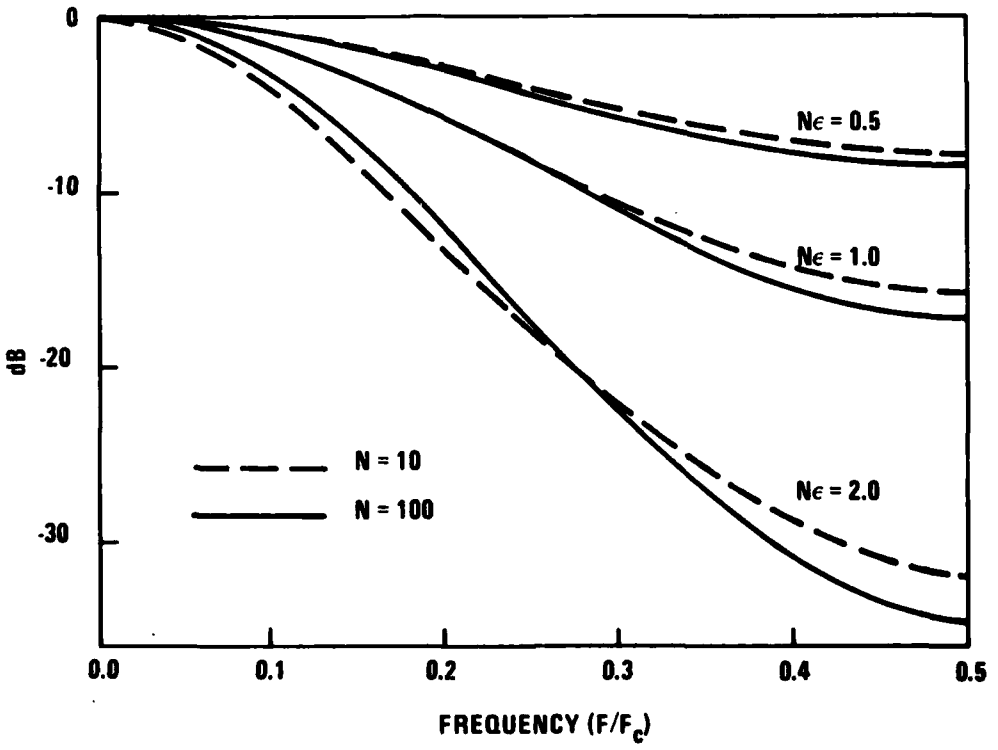


Figure 13. Frequency Response of CCD Delay Lines for Various Transfer Inefficiencies and for 10 or 100 Stages

Stop-Band

Analysis of effects in the stop-band is best performed via the z-transform. This shows that the effect of transfer inefficiency is to move the zeros away from the unit circle. This warping of the frequency response can be seen intuitively as follows: A nonzero transfer inefficiency delays the passage of input charge packets down the CCD and so reduces the velocity of the input sine wave, if considered as a wave on the surface of the CCD. So, for a given input frequency, the wavelength will be shorter. Since the filter structure responds to wavelength rather than frequency the filter will give an output amplitude corresponding to a higher frequency; thus the frequency response will be distorted along the frequency axis, each point being moved a distance

$$\left(\frac{F_c}{2\pi}\right)\epsilon \sin\left(\frac{2\pi F_{sig}}{F_c}\right)$$

SIMULATION OF THE COMPLETE FILTER

Figure 14 shows the frequency responses of the 63-tap filter for $N\epsilon/2 = 0.1$, 0.3, and 1.0. As can be seen as $N\epsilon$ increases, the minima in the stop-band become less sharp, the maxima are reduced, and the response tends to move towards higher frequencies. A droop in the pass-band is also apparent, as predicted by the results shown in Figure 13.

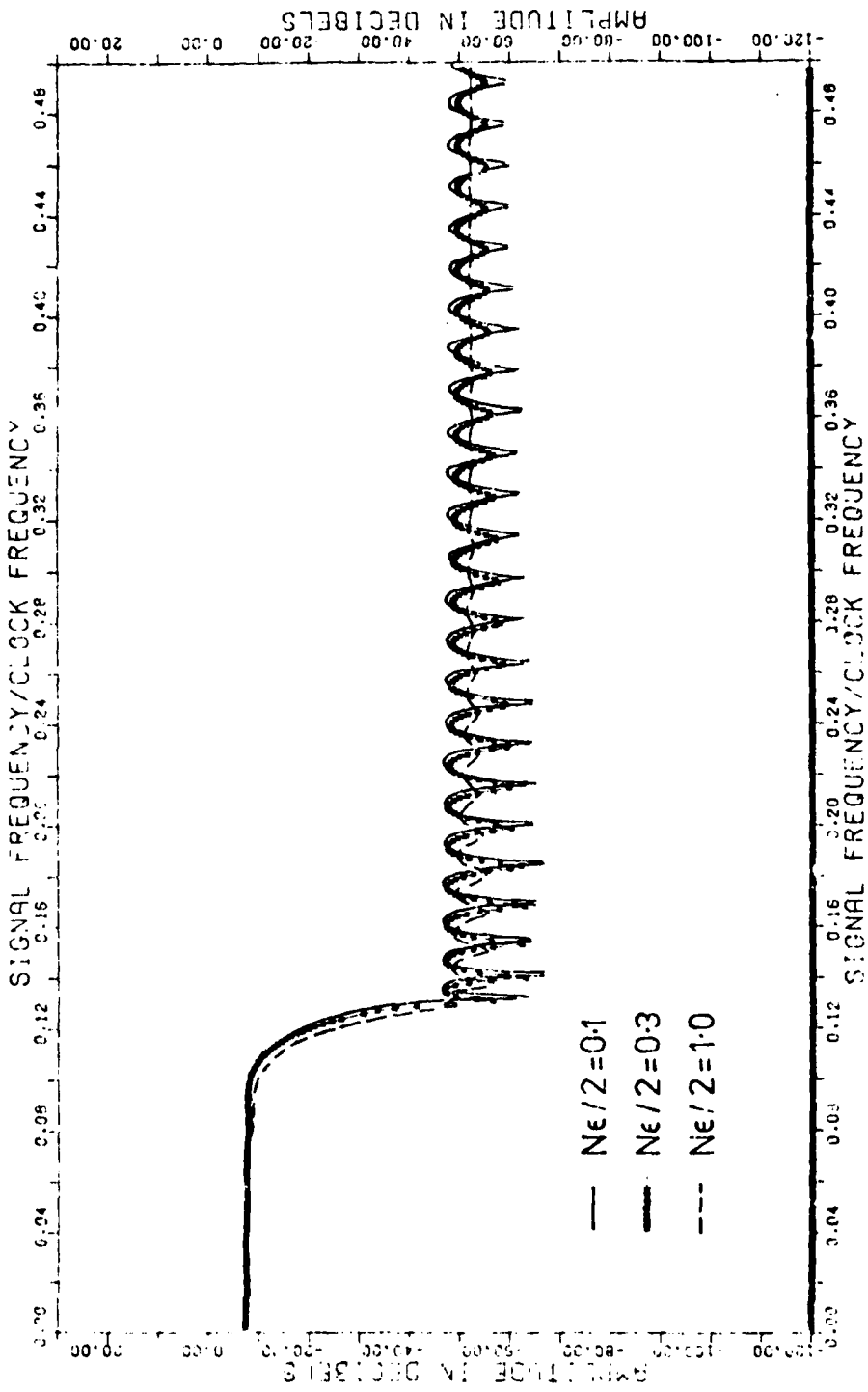


Figure 14. Degraded Frequency Responses of Filter for Various Nε

CORRECTION OF TRANSFER INEFFICIENCY EFFECTS

As we have discussed above, charge transfer inefficiency (CTI) in CCD transversal filters leads to degradation of the filter impulse response. Although the average CTI is not known in advance of a filter processing run, we can ask whether or not the impulse response of the filter can be pre-distorted to nullify the distortion caused by CTI. The answer to this question has been "yes" in the literature.[3] Below we analyze the question in more detail.

A CCD delay cell is assumed to have the model shown in Figure 15a. The single-stage transfer function is given by:

$$\lambda(Z) = \left(\frac{(1 - p\epsilon)Z^{-1}}{1 - p\epsilon Z^{-1}}\right)$$

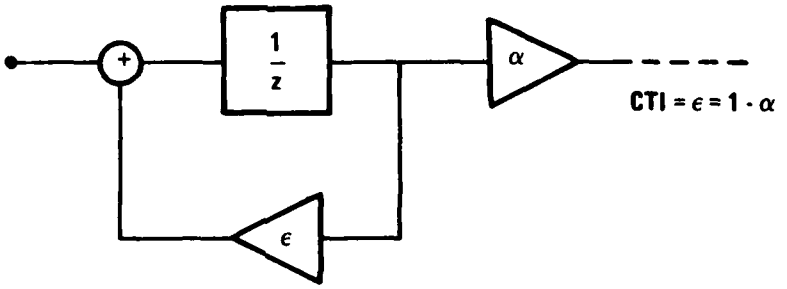
where p is the number of phases per bit.

An N-stage filter can be constructed from the single stages, as shown in Figure 15b. The total transfer function is given by:

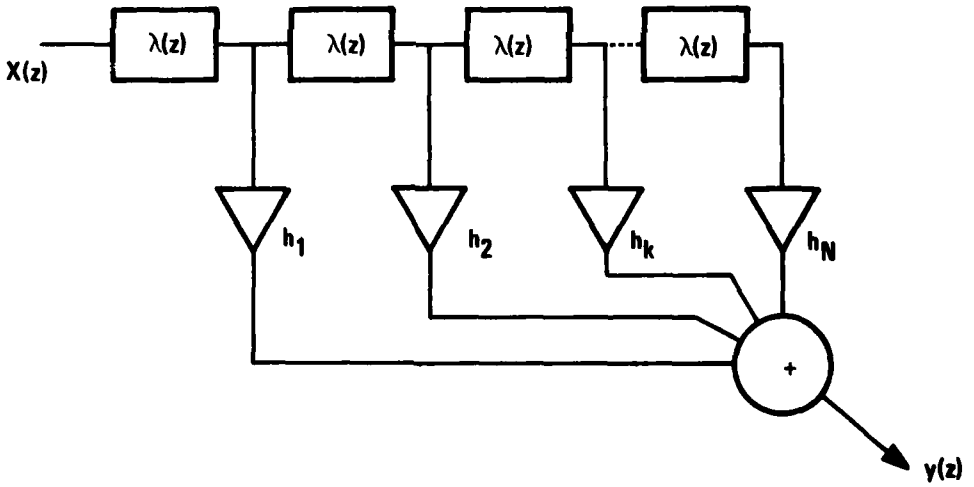
$$H'(Z) = \frac{Y(Z)}{X(Z)} = \sum_{i=1}^{N} h_i \lambda(Z)^i = \sum_{i=1}^{N} h_i \left(\frac{(1 - p\epsilon)Z^{-1}}{1 - p\epsilon Z^{-1}}\right)^i$$

If our desired transfer function is

$$H(Z) = \sum_{i=1}^{N} h_i Z^{-i}$$



a. CCD delay cell



b. N-stage CCD filter

Figure 15. Models of CCD Filters

then we would like to find a set h_i' such that

$$H(Z) = \sum_{i=1}^{N} h_i' \lambda(Z)^i = \sum_{i=1}^{N} h_i' \left(\frac{(1 - p\epsilon)Z^{-1}}{1 - p\epsilon Z^{-1}} \right)^i$$

If we equate the two sides and solve for h_j', we obtain:

$$h_j' = \frac{\left\{ h_j - \sum_{i=1}^{j-1} h_{j-i}' \binom{J-1}{i} p\epsilon^i (1 - p\epsilon)^{j-i} \right\}}{(1 - p\epsilon)^j}$$

There are several difficulties with such an expression. First, the assumption is that all the ϵ are identical and independent of the clocking mechanism. In practice, however, ϵ is a function of signal charge packet size and is not only variable among stages but may not be constant among phases, either. In other words, if clocking of a four-phase filter, for example, is done in two-and-a-half phase fashion, the simple model of Figure 15a may not be valid. A second major difficulty with the derivation above is that we often do not know ϵ in advance. We are examining not only more detailed modeling of the charge transfer process, but also the optimum way to correct for CTI without prior CTI information.

SECTION 3

DESIGN AND MODELING OF CCD AND SWITCHED-CAPACITOR (SC) RECURSIVE FILTER STRUCTURES

The various CCD and SC structures under investigation are sufficiently simple that programs on HP67/41C calculators can be used. The following description outlines the device and system structures and gives appropriate examples of the use of the HP67/41C programs.

GENERAL SCCD PROBLEMS (PRGM: FGTAP)

The analysis and design of surface-channel devices requires, at least, a solution to the one-dimensional poisson equation with the depletion approximation. Three subroutines are needed to give a complete description of the SCCD:

a. Computation of surface potential, ψ_s, for arbitrary gate-substrate voltage with arbitrary channel charge.

b. Computation of channel charge, Q_s, for arbitrary gate-substrate voltage with arbitrary surface potential.

c. Computation of change in floating-gate voltage, ΔV_{FG}, for arbitrary initial voltage, V_G^0, with arbitrary single-channel charge injection and arbitrary capacitive loading, C_s, of the single floating gate.

There is a slightly more complex problem, which generally exists in practice where a Reset MOST is used to define the initial voltage. This problem has a different (but similar) solution to the charge balance equation to account for leakage current flow from the floating gate during the sensing time interval. This has not yet been used although the analysis has been performed.

The three equations which are solved for the above are (N-channel):

$$\psi_s = V_G^1 + V_o - \left[V_o^2 + 2V_o V_G^1\right]^{1/2} \tag{1}$$

$$Q_s = A\,C_{ox}\left\{(\psi_s - V_G + V_{FB}) + (2V_o\psi_s)^{1/2}\right\} \tag{2}$$

$$\Delta V_{FG} = V_G^Q - V_G^0, \text{ the change in gate volts} \tag{3}$$

$$= \frac{-\beta + \sqrt{\beta^2 - 4\gamma}}{2}$$

where

$$\beta = 2\left(\frac{A}{C_s}\right)\left\{\frac{Q_s}{A} + C_{ox}\left(V_o^2 + 2V_o[V_G^0 - V_{FB}]\right)^{1/2} + \left(\frac{A}{C_s}\right)C_{ox}^2 V_o\right\} \tag{4}$$

$$\gamma = \left(\frac{A}{C_s}\right)^2\left\{\left[\frac{Q_s}{A} + C_{ox}\left(V_o^2 + 2V_o[V_G^0 - V_{FB}]\right)^{1/2}\right]^2 - C_{ox}^2\left(V_o^2 + 2V_o\left[V_G^0 - V_{FB} + \frac{Q_s}{AC_{ox}}\right]\right)\right\} \tag{5}$$

The physical parameters are contained in:

$$V_G^1 = V_G - V_{FB} + \frac{Q_s}{AC_{ox}}$$

$$V_o = q \epsilon_s \epsilon_o N_A / C_{ox}^2$$

Q_s = total channel charge

A = active channel-gate area

C_{ox} = oxide capacitance per unit area

C_s = total constant load capacitance

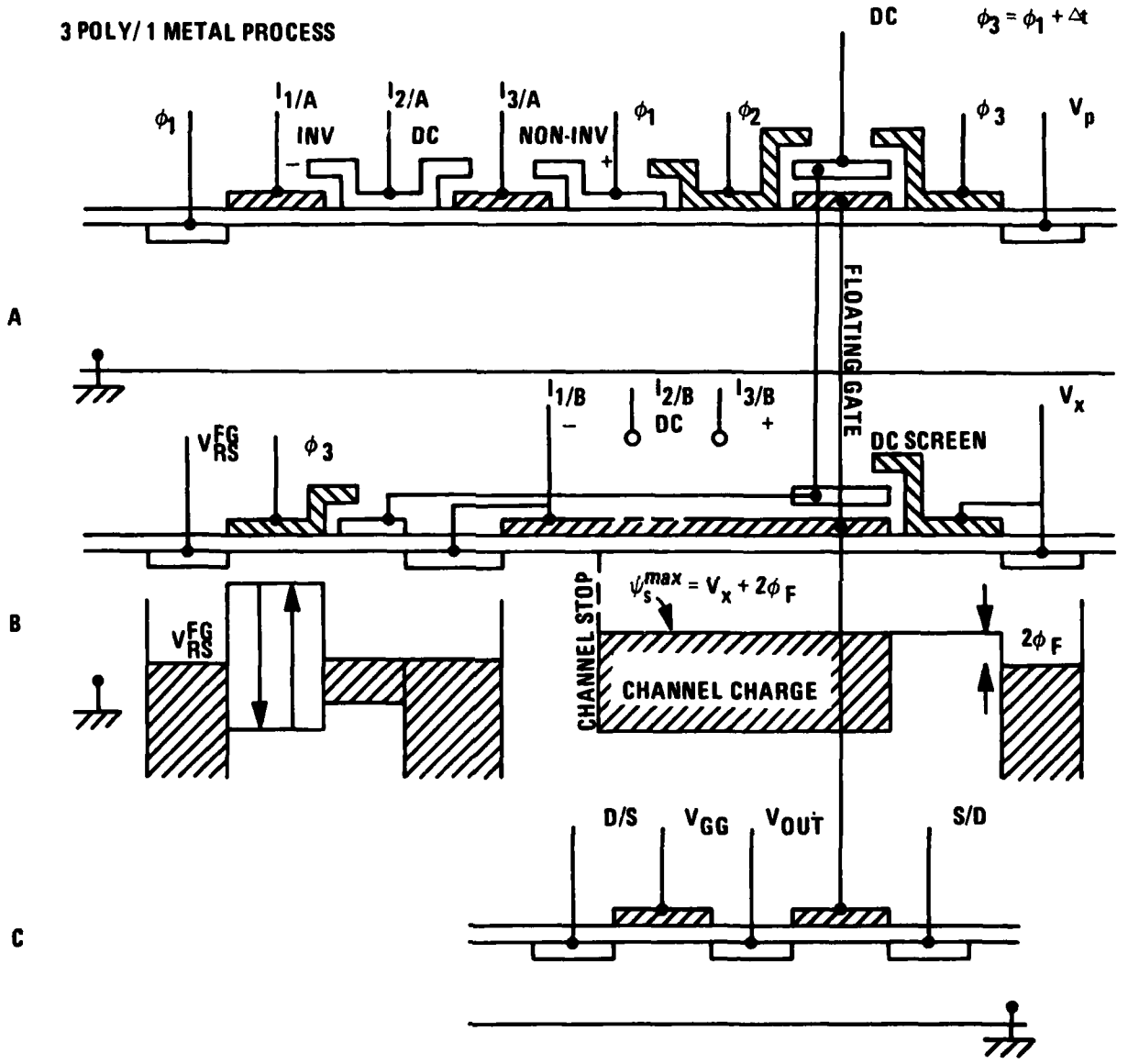
V_{FB} = flat-band voltage

Since the floating-gate Equation (3) is explicit for large signals the program also provides the value of the slope of the transfer function at any value of signal charge:

$$\frac{\delta \Delta V_{FG}}{\delta Q_s} = \left[\frac{1}{A} \frac{\delta \Delta V_{FG}}{\delta \beta} \cdot \frac{\delta \beta}{\delta Q_s} + \frac{\delta \Delta V_{FG}}{\delta \gamma} \cdot \frac{\delta \gamma}{\delta Q_s} \right]$$

Using subroutines a) and b) in sequence gives a direct calculation of charge-handling capability and also input voltage-to-charge sensitivity.

Figure 16 shows a cross-section of the surface-channel test structure showing the three major components. The new feature is the voltage-controlled capacitance load, V_x, which is used to set the sensitivity of the floating gate. Figure 17 shows the expected behavior of this capacitance with voltage and Figure 18 shows the resulting effect on the floating-gate response.



A = INPUT-SUMMING DELAY UNIT $\approx 20000\ \mu m^2$

B = ELECTRICALLY-PROGRAMMABLE CAPACITANCE LOAD $\approx 4500\ \mu m^2$

C = OPTIONAL BUFFER $\approx \frac{1800\ \mu m^2}{26300\ \mu m^2}$

(162 x 162 μm)

Figure 16. Cross-Section of SCCD Test Structure

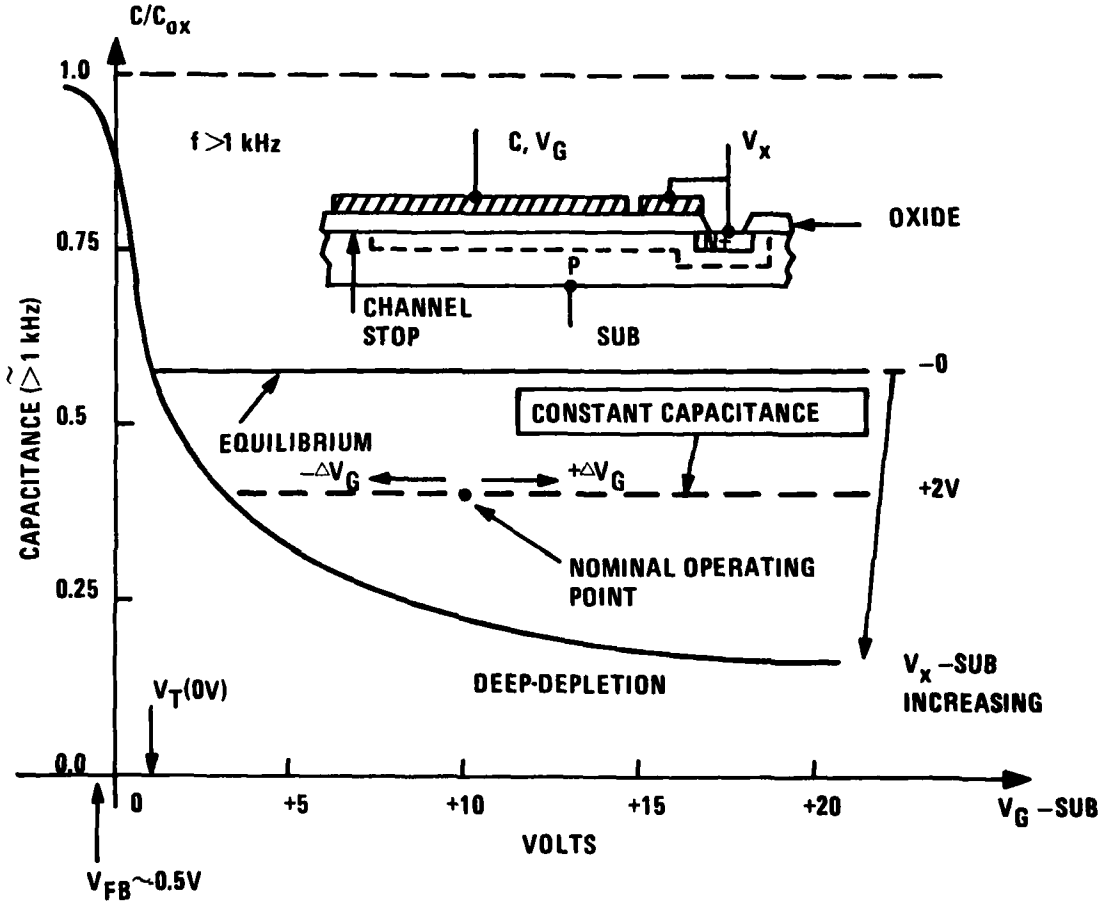


Figure 17. Expected HF Behavior ($\gtrsim$ 1 kHz) of Capacitance with Gate Voltage (V_x variation selects a new value of constant capacitance.)

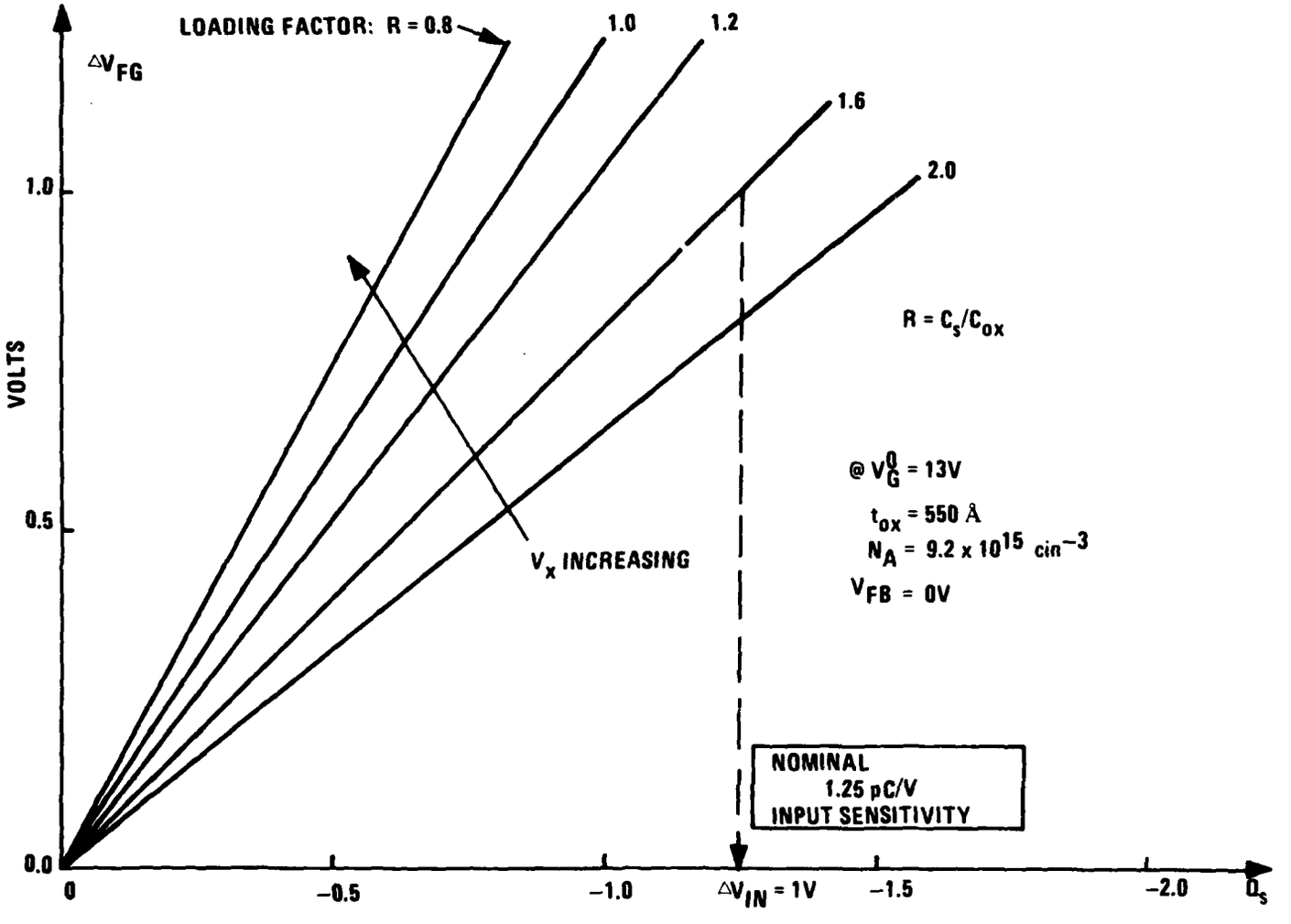


Figure 18. Calculated Floating-Gate Response

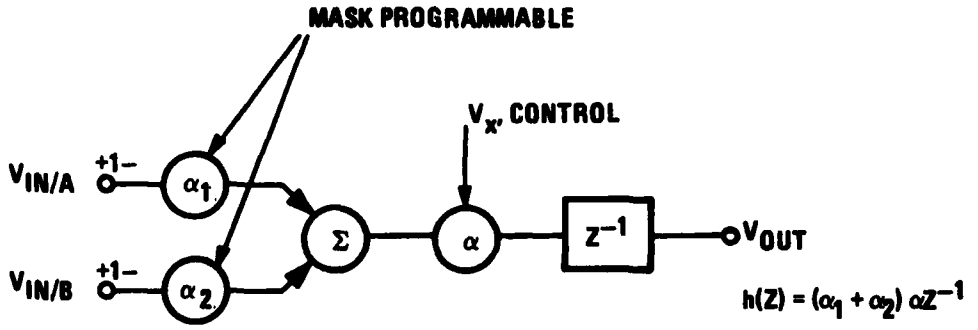
The structure consequently allows a programmable range of linear response which may be used to construct a multiply-delay-sum function. There are several applications of such a function, as shown in Figure 19. A photograph of the actual test structure in first-order low-pass form is shown in Figure 20; the total area can be compared to the 4 x 3 mil^2 pads.

The consequences of using a given structure are under study. For the present, the basic performance of the test structure will be compared to that predicted to get a data base for predicting high-order filter performance. In particular, transfer inefficiency residuals should be a small error since the number of transfers is a minimum. The HP67/41C program does not, as yet, contain second-order effects such as this, but our more complete FORTRAN programs do allow second-order effects to be studied.

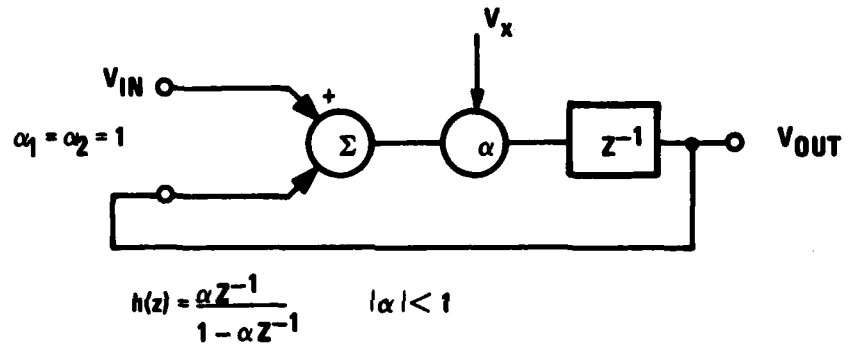
SC TEST STRUCTURE

The main objective of this structure is to produce a transfer function of band-pass type without the use of an operational amplifier. Charge gain is obtained by discharging an input capacitor (or capacitors) through a MOST current mirror and thereby causing a controlled discharge of a different capacitor connected to the output of the current mirror.

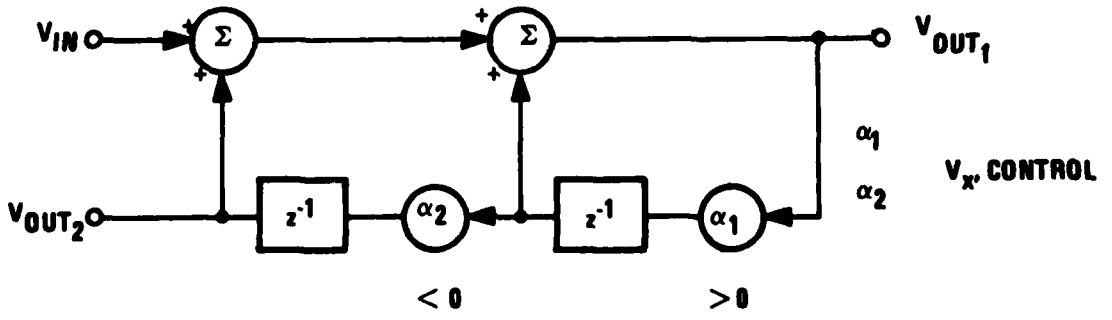
By using two stages of current mirror with four-phase clock pulses it is possible to cancel out the first-order offsets due to threshold voltage ($V_T \neq 0$) and pre-charge voltage ($V_{DD} \neq 0$) residuals on the capacitors.



a. General structure of multiply-delay-sum



b. First-order recursive low-pass



$h_1(z) = [1 - \alpha_1 z^{-1} - \alpha_1 \alpha_2 z^{-2}]^{-1}$ (INDIRECT)

$h_2(z) = \alpha_1 \alpha_2 z^{-2} [1 - \alpha_1 z^{-1} - \alpha_1 \alpha_2 z^{-2}]^{-1}$ (DIRECT)

c. Second-order recursive band-pass

Figure 19. Applications of Multiply-Delay-Sum Function

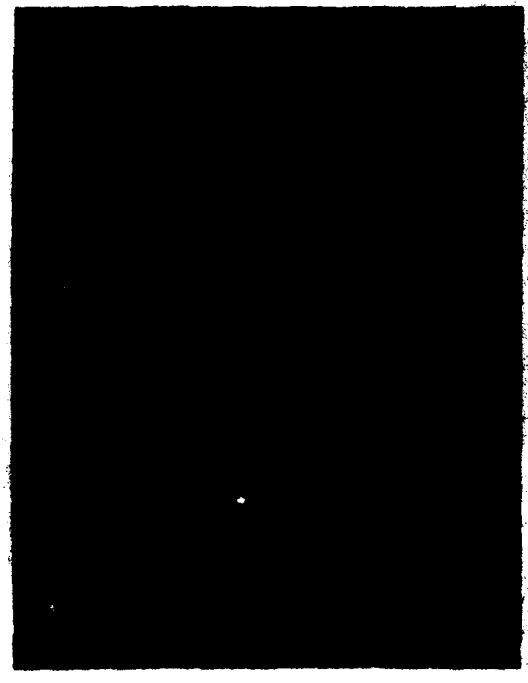
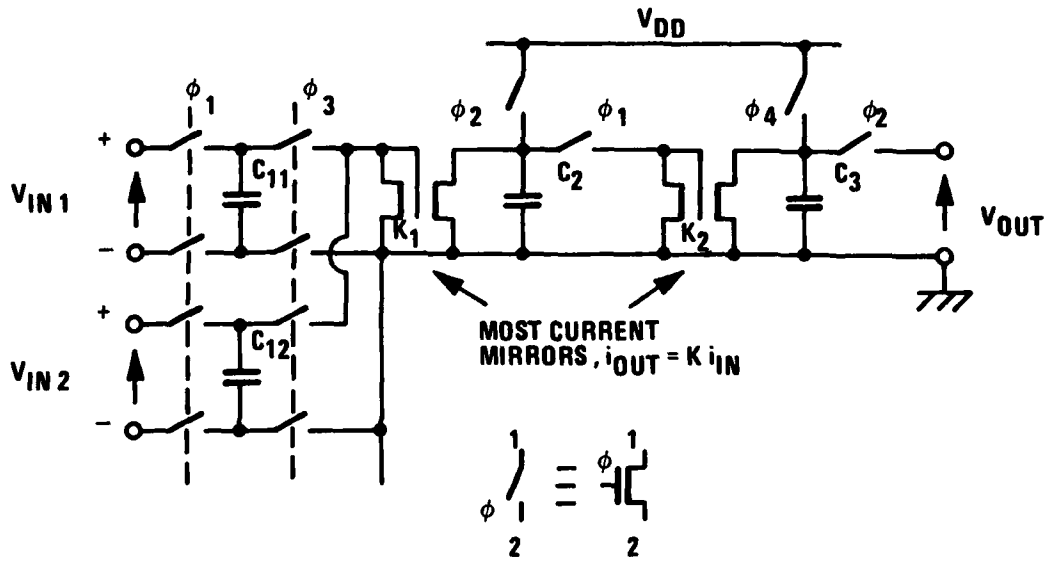


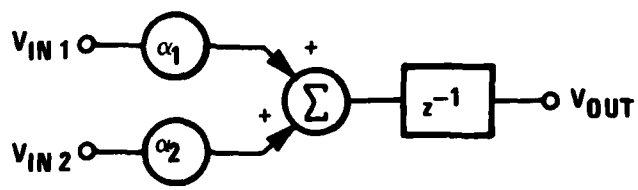
Figure 20. Photograph of the SCCD Test Structure (The V_x control is on the top right.)

A simple charge-domain analysis of the circuit shown in Figure 21 results in the transfer function at the beginning of phase two:

$$h(Z) = V_{DD}\left(1 - K_2 \frac{C_2}{C_3}\right) + V_T K_2 \frac{C_2}{C_3}\left(1 - K_1\left(\frac{C_{11} + C_{12}}{C_2}\right)\right) + \frac{K_1 K_2}{C_3}\left(C_{11} V_{IN1} + C_{12} V_{IN2}\right) Z^{-1}$$



a. Circuit diagram of SC section. Clock phases are mutually exclusive and follow index sequence.



b. Z-domain equivalent of a.

Figure 21. Switched-Capacitor Realization of Multiply-Delay-Sum Function

This analysis was first published by Arreola, et al., in Electronics Letters, Vol. 15, No. 24, November 22, 1979.

The transfer function is similar to that for the SCCD test circuit except that the multipliers of the input voltages are constrained such that they sum to unity; that is:

$$V_{OUT}(Z) = \alpha_1 V_{IN} Z^{-1} + \alpha_2 V_{IN} Z^{-1}$$

where

$$\alpha_1 = \frac{K_1 K_2}{C_3} C_{11}$$

$$\alpha_2 = \frac{K_1 K_2}{C_3} C_{12}$$

However, for cancellation of the offsets

$$K_1 = \frac{C_2}{C_{11} + C_{12}}, \qquad K_2 = \frac{C_3}{C_2}$$

Thus

$$\alpha_1 = \frac{C_{11}}{C_{11} + C_{12}}$$

$$\alpha_2 = \frac{C_{12}}{C_{11} + C_{12}}$$

Therefore

$$\alpha_1 + \alpha_2 \equiv 1$$

And furthermore

$$\alpha_i \geq 0$$

The SC has the major advantages of being large signal and infinitely extendable with extra input capacitors C_{1x}. We have designed a single-input capacitor structure with current mirror ratios

$$K_1 = 1/2, \quad K_2 = 1$$

so that a direct measurement of the offsets can be made easily. The values of K are mask programmed by designing the current mirror with duplicate transistor pairs. Connecting two on the input side and one on the output gives the "half" and similarly for unity. Since fabrication tolerances should be identical, an accurate measurement of mirror tracking should be possible as a function of frequency. The capacitors are designed to be identical and are implemented by Poly I and Poly II capacitors with "zero" overlap. The capacitance values, of course, depend on the oxide thickness and on the absolute area but, to first order, differences should be negligible. Parasitic loading due to the transistor drain/source junctions will limit the linearity of the transfer function since they are "square law" with voltage. It should be possible to measure the distortion due to that effect on the present structure. Signal lines are screened throughout by using a Poly II shield between Poly I gate and first-level metal.

A photograph of the structure is shown in Figure 22, where C_1 is on the left. The structure is arranged to butt at left/right for higher-order sections. As can be seen, the section is very compact with the small capacitors used. The ideal transfer function of a first-order section is shown in Figure 23, for three values of α_1. The phase response is not quite linear, but since the multipliers must sum to unity the section is unconditionally stable.

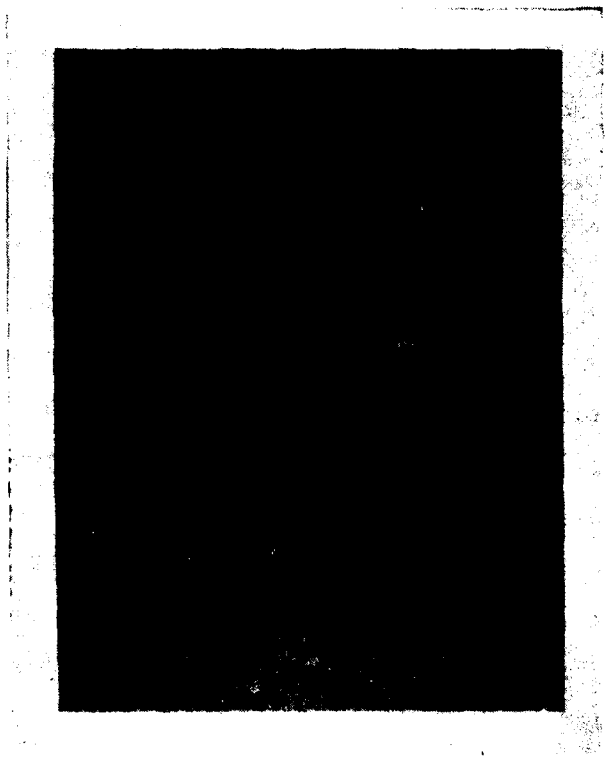


Figure 22. Photograph of the SC Test Structure

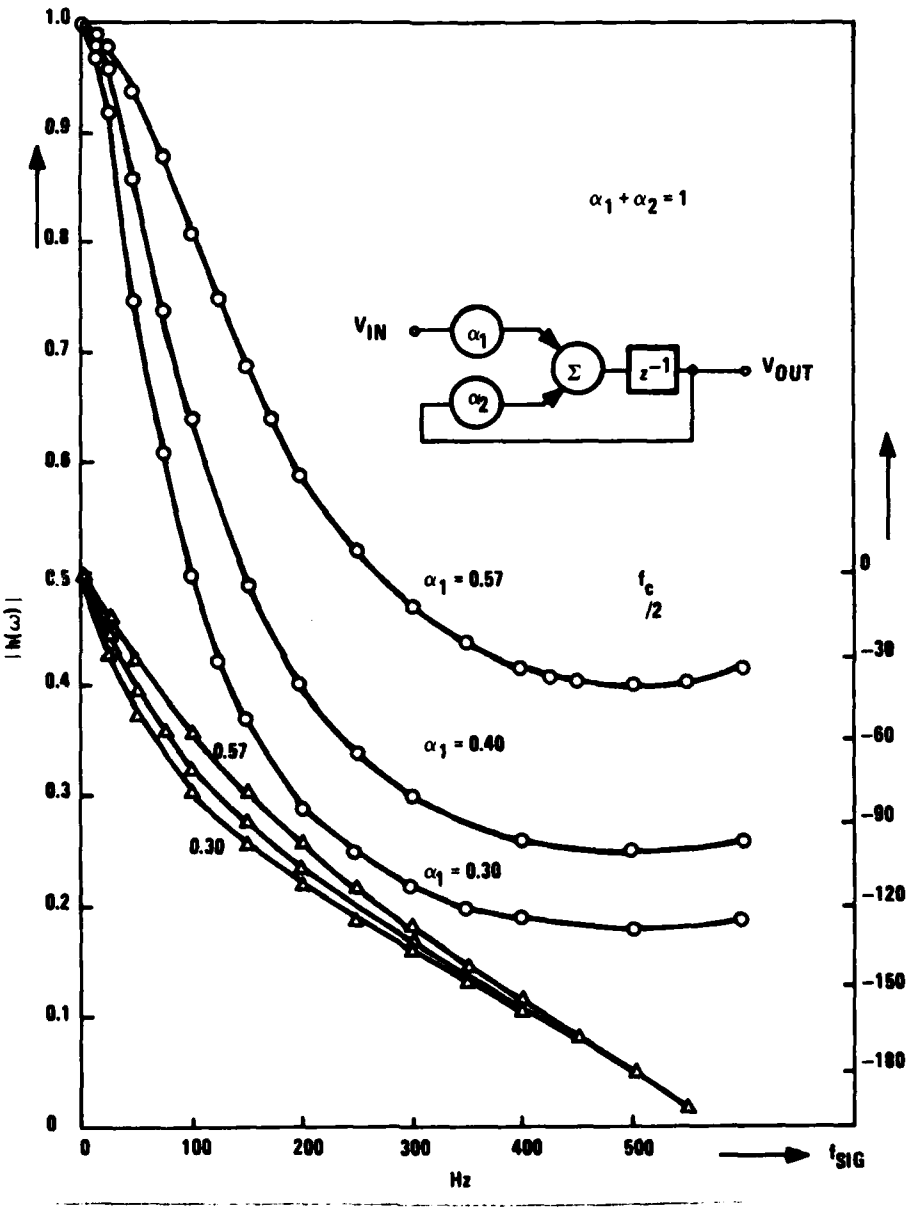


Figure 23. First-Order Recursive Low-Pass Filter

REFERENCES

1. Traynar, C.P., Beynon, J.D.E., Roberts, P.C.T. and Pennock, J.L., "Depletion-Capacitance-Induced Distortion in Surface-Channel CCD Transversal Filters," IEE J. Solid State and Electron Devices, 1, 73, 1977.

2. Hense, K.R. and Collins, T.W., "Linear Charge-Coupled Device Signal Processing Techniques," IEEE Trans., Vol. ED-23, No. 265, 1976.

3. Broderson, R.W., Hewes, C.R. and Buss, D.D., "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE J. Solid State Circuits, Vol. SC-11, No. 75, 1976.

4. Sequin, C.H., et al., "Self-Contained Charge-Coupled Split-Electrode Filters Using a Novel Sensing Technique" IEEE J. Solid-State Circuits, Vol. SC-12, No. 626, 1977.

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